VIT®
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

School of Electronics Engineering

Department of Micro and Nano Electronics

Cordially invites you for

One-day Workshop

on

An Interactive FPGA SoC Design Workshop

29th March 2025 (9:00 AM – 5:00 PM)

Venue: TT237A(FN), and TT727(AN)

Who Can Attend

Students (B.Tech and M.Tech)

Research Scholars

Faculty

Resource Person

Dr. Antony Xavier Glittas X,

Dr. Vetriveeran Rajamani, Asso. Prof. Grad. 1,

VIT University, Vellore

Chairperson

Dr. Jasmin Pemeena Priyadarisini,

Professor & Dean, SENSE.

Convenor

Dr. Sriadibhatla Sridevi,

Professor & Head,

Department of Micro & Nano Electronics,

SENSE.

Coordinators

Dr. Antony Xavier Glittas, Asst. Professor Sr.,

Dr. Vetriveeran Rajamani, Asso. Prof. Grad. 1,

Department of Micro & Nano Electronics,

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An E-certificate will be provided to all the participants

Agenda

Session	Topics
Session 1 (09:00 AM – 10:30 AM)	➢ Introduction to FPGA SoC Architectures ➢ Vivado Design Flow using PYNZ Z2 SoC
Session 2 (10:45 AM – 12:30 PM)	➢ Vivado Block design example ➢ Custom Block design
Session 3 (1:30 PM – 3:00 PM)	➢ PYNQ Z2 overlay ➢ Loading the bitstream & device tree setup ➢ Writing Python APIs for overlay interaction in Jupyter Notebook
Session 4 (3:15 PM – 5:00 PM)	➢ Implementation of the AI algorithm in the ZYNQ PS system ➢ Vitis HLS Design Flow: C++ to Hardware