VIT®

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

## School of Electronics Engineering (SENSE)

**Department of Micro & Nano Electronics**

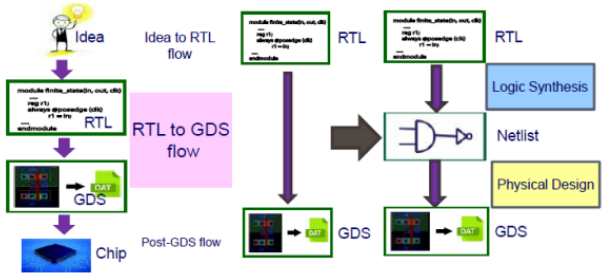
**Offers**

## Value Added Course

**on**

# VAC2336 RTL to GDSII

## (SYSTEM ON A CHIP DESIGN)




**19th Jan, (8, 16, 23) Feb & 9th March, 2025**

## About Training:

With today's increasingly large and complex digital IC and system-on-chip (SoC) designs, design power closure, circuit power integrity and Testing become one of the main engineering challenges, thereby impacting the device's total time-to-market. This Training will teach you how to implement a design from RTL-to-GDSII using various industry standard tools. You will start by coding a design in Verilog, simulate, synthesize and optimize for a better design.

## Who Can Attend?

➔ VIT Students –UG/PG [M.Tech ( VLSI Design) exempted].

## Key Benefits:

This course is designed to introduce the engineers to the area of specification to chip design. The candidates who successfully undergo this training would be able to design a digital system optimized in terms of area, power and timing by applying appropriate constraints. It enable them to apply all possible Power minimization and DFT techniques to build a more reliable system. It provides them an opportunity to carry out the industry standard projects from specification to GDSII.

## Last date for Registration:

On or before : 15th January 2025

## Course Fee:

**Registration Fee:** VIT Student: **Rs.500/-**
(Inclusive of GST)

Course Material and projects will be provided to all.

***Certificate will be issued for those students who have 75% attendance and 50% Marks in the evaluation)***

## Course Content:

- FSM Coding Guideline and Coding Style for Synthesis
- Architecture of Logic Synthesizer
- Synthesis Optimization- Timing Parameter Definition – Setup and Hold Timing Check
- Multicycle Paths- Half-Cycle Paths- False Paths.
- Low Power Synthesis, DFT Based Synthesis.
- Pattern Generation- Fault Simulation – Scan Chain Insertion- Fault Coverage.
- Floor plan, Placement, CTS and routing– ECO flow – Signal Integrity Issues,
- Timing Sign-off, Physical Verification
- Mini Project.

## Convener:

**Prof. S. Sivanantham**
Dean, School of Electronics (SENSE)

## Co-Convener:

**Prof. Jagannadha Naidu K**
HoD, Department of Micro & Nano Electronics

## Coordinators:

➔ **Dr. Sakthivel Ramachandran**
Professor

➔ **Dr. Jagannadha Naidu K,**
Associate Professor

## For Registration contact:

**Mr.V.Karthikeyan**
Contact No.: 9894972399

## Registration Venue:

Technology Tower: TT237

## Event Venue:

TT238, Technology Tower

## Online Payment link

Link: Link: https://events.vit.ac.in/

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# VAC2336 RTL to GDSII

**(SYSTEM ON A CHIP DESIGN)**

## SCHEDULE FOR VAC

| Date | Timing | Topics & Faculty |
|---|---|---|
| Sunday (19/01/2025) | 9.30-11.15AM | Coding Style for Synthesis- Prof.Sakthivel |
| | 11.30-12.45PM | FSM Coding Guideline- Prof.Sakthivel |
| | 2.14-3.30PM | Architecture of Logic Synthesizer , Basics of STA- Prof.Jagan |
| | 3.30-5.00PM | Mini Project Spec discussion for implementation- Prof.Jagan &Sakthivel |
| 8/2/25 Saturday | 9.30-11.15AM | Basics of Testing Pattern Generation- Fault Simulation &FC, Prof.Sakthivel |
| | 11.30-12.45PM | DFT Based Synthesis, LBIST & MBIST- Prof.Sakthivel |
| | 2.14-3.30PM | Lab: Combinational circuit, Test pattern generation, FC etc- Prof.Jagan &Sakthivel |
| | 3.30-5.00PM | Lab for Logic Synthesis & STA - Prof.Jagan &Sakthivel |
| 16/2/25 Sunday | 9.30-11.15AM | Floor plan, Placement, CTS and routing- Prof.Jagan |
| | 11.30-12.45PM | ECO flow – Signal Integrity Issues- Prof.Jagan |
| | 2.14-3.30PM | Lab- Prof.Jagan &Sakthivel |
| | 3.30-5.00PM | Lab- Prof.Jagan &Sakthivel |
| 23/2/25 Sunday | 9.30-11.15AM | Industry Expert Lecture |
| | 11.30-12.45PM | Industry Expert Lecture |
| | 2.14-3.30PM | Lab: DFT Synthesis, scan chain insertion and analysis- Prof.Jagan &Sakthivel |
| | 3.30-5.00PM | Project implementation and discussion |
| 9th March, 2025 | 9.30-11.15AM | Exam- Prof.Jagan &Sakthivel |
| | 11.30-4.30PM | Mini Project Evaluation- Prof.Jagan &Sakthivel |
| | 4.30-5.00PM | Feedback & closing ceremony |

Prerequisite: We request all participants to refresh your Verilog programing skill with digital circuits. (Both combinational and sequential circuits)