ONLINE INTERNSHIP TRAINING PROGRAM
On
Hardware for Computational Neuroscience

Date: 26th April-2021

Course Description:

This is a online, instructor – led course which provides a thorough knowledge about the Hardware for computational neuroscience. Two Weeks online training with Remote FPGA Lab Access for the candidates. Well Experienced Faculties from Vellore Institute of Technology – (VIT Vellore) and National Institute of Electronics and Information Technology- (NIELIT Calicut) will be handling the sessions for all the 10 Days.

Program Objectives

To learn, Practice- FPGA Design Flow and Hardware for computational neuroscience. To get exposure in industry standard methodologies .

Who can attend?

Students of Engineering (UG & PG) & MSc (Electronics), PhD scholars, faculty members and professionals from Industry**.**

Duration

- Proposed length of the training: 10 Days. 20 Hours lecture 30 Hours practicals.

Course Fee
INR 4,000/- For Students **INR 5,000/- For Faculty** REGISTER NOW **INR 8,000/- For Industry/Corporate** **Last date for payment and confirmation: 23rd April 2021**

Payment Guidelines: -

Online fund transfer can be made via your Internet Banking, Google Pay to the following account and proof of the same has to be uploaded during the registration.

Account details:

Name of the Institute: National Institute of Electronics and Information Technology, Calicut.
Account Holder: Director NIELIT Calicut

Account No: 10401158037 Bank Name: SBI, NIT Chathamangalam

IFSC No: SBIN0002207 MICR Code: 673002012

For any queries WhatsApp to 9447769756, Please don't call, we will reply to you at the earliest.

Delivery Mode: Online. Live classes followed by online assignments over LMS. Students should have Laptop/PC with high speed internet connectivity.

Tentative Schedule

Duration	:	2 weeks
Tentative Timings	:	10 am to 12.00 noon (Theory) Lab/Assignments can be submitted online on Leaning management Systems (Any Time)
Tentative dates	:	26th April 2021 to 7th May 2021

Syllabus

	Theory	LAB	Faculty (Indicative)
Day 1	Verilog HDL	Mentor Graphics or Xilinx Vivado Simulation	NIELIT Calicut
Day 2	FPGA Design Flow-1	Xilinx Vivado	NIELIT Calicut
Day 3	FPGA Design Flow-2	Xilinx Vivado	NIELIT Calicut
Day 4	FPGA Design Flow- IP Cores	Xilinx Vivado	NIELIT Calicut
Day 5	FPGA Design Flow- Advanced	Xilinx Vivado	NIELIT Calicut
Day 6	Neurons and Spiking Neural Networks, Brain as a potential Technology	Xilinx Vivado	VIT Vellore
Day 7	Artificial Neural Networks in Hardware	Xilinx Vivado/ LT spice(Open source)	VIT Vellore
Day 8	Hardware implementation of Spiking Neural Networks	Xilinx Vivado/ LT spice(Open source)	VIT Vellore
Day 9	Programmable and configurable Analog Neuromorphic IC	Xilinx Vivado/LT spice(Open source)	VIT Vellore
Day 10	Understanding Neuromorphic System and Building Neuromorphic System	Xilinx Vivado	VIT Vellore

Certificate: e-Certificate will be mailed to the registered email address after completion of the course.

Course Materials

Lectures Notes will be given to each participant via email/WhatsApp

Coordinators

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