About the Institution

VIT was established with the aim of providing quality higher education on par with international standards. The global standards set at VIT in the field of teaching and research spur us on in our relentless pursuit of excellence. In fact, it has become a way of life for us. The highly motivated youngsters on the campus are a constant source of pride. Many of our students, who pursue their research projects in foreign universities, bring high quality to their work and esteem to India and have done us proud. With steady steps, we continue our march forward. We look forward to meeting you here at VIT.

About the SCHOOL OF ELECTRONICS (SENSE) School

SENSE at VIT was established for imparting state-of-the-art knowledge in Electronics and Communication Engineering, VLSI and allied areas. B.Tech. Electronics and Communication Engineering is accredited by the Engineering Accreditation Commission of ABET, http://www.abet.org. Faculty are actively involved in R&D activities and are working on research projects funded by government organizations like DRDO, ISRO (RESPOND), BRNS and agencies like DST.

About the Micro and Nano Electronics (MNE) Department

MNE students are in great demand in various core companies like Intel, Texas Instruments, Cadence, ARM, Open Silicon, ST Microelectronics, MediaTek, Qualcomn, Synopsis, Xilinx, NXP Semiconductors etc

CHIEF PATRON

Dr. G.Viswanathan, Chancellor, VIT, Vellore

PATRONS

Mr. Sankar Viswanathan, Vice President

Dr. Sekar Viswanathan,Vice President

Dr. G.V.Selvam , Vice President

Dr. Rambabu Kodali , Vice Chancellor

Dr. Partha S Mallick, Pro Vice Chancellor

Dr. Jayabarathi , Registrar

CONVENORS

Dr. S.Sivanantham .S, Professor & Dean

Dr. Jagannadha Naidu K , HOD,MNE

COORDINATORS

Dr. Ravi S, Associate Professor

Dr. Sakthivel Ramachandran , Professor

Registration Link

Registration is compulsory for the participant so kindly register before 20th Nov 2023.

(Registration Limited to 50 Participants on First come First Serve Basis)

For Registration use the following link

https://atalacademy.aicte-india.org/signup

Registration ID : 1691730133

https://tinyurl.com/y2nn5m92

VIT®

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

AICTE ATAL

Sponsored offline FDP

Silicon to Chip Design

(Si2Chip)

11 – 16 December 2023

COORDINATORS

Dr. Ravi S

Dr. Sakthivel Ramachandran

Organized by

Department of Micro and Nano electronics (MNE)

School of Electronics Engineering (SENSE)

Vellore Institute of Technology (VIT)

Vellore-632014

AICTE Training and Learning (ATAL) Academy

AICTE Training and Learning (ATAL) Academy, established by MOE, Government of India, holds the vision to empower faculty to achieve goals of higher education such as access, equity and quality. Council understands that there is a need of the day to train the young generation in skill sector and having faculty & technicians to be trained in their respective disciplines with latest tools and technologies.

The main objective of ATAL Academy is to plan and help in imparting quality technical education in the country and to support technical institutions in fostering research, innovation and entrepreneurship through training in various emerging areas. It also provides a variety of opportunities for training and exchange of experiences such as workshops, orientations, learning communities, peer mentoring and other FDPs.

Discussion Planned

Introduction to Semiconductor Device Physics
Device Modeling – LAB (Synopsys-TCAD)
Life of CMOS Design
FinFET in IC Design & Challenges in 5nm & 7nm node.
Schematic to Layout - LAB (Cadence Virtuoso) -
Logic Design using HDL
HDL Based FSM Design for real-time applications + FPGA Implementation
Gate level Simulation - LAB (Cadence NC Sim & genus)
Design for Testability and its Challenges
Low Power and DFT based Synthesis-LAB (Cadence genus & Modus) , Quiz1
Design for Testability and its Challenges
Physical Design and its Challenges in Deep submicron nodes – Cadence Innovus
STA for Nanometer design
AI / ML Applications in Chip Design

Objectives of the Programme

The primary goal of the FDP is to promote research and developmental activities to solve problems related to Advanced VLSI (Chip) Logic Design, Physical Design in current VLSI semiconductor era. This creates an opportunity to equip with the ongoing Technological development in the area of VLSI and IoT. The program is intended to provide a vibrant opportunity for VLSI design.

Experts involved.

Dr.Harish M Kittur , Professor , VIT.
Dr.Lakshmi Narayanan , NIT, Trichy.
Dr.Noor Mohammad , Asso .Professor, IIIT Kanchipuram.
Dr.Ramakrishnan,Professor, VIT.
Dr.Ramkumar ,Director,RAMIC Solutions.
Mr.Murugeswaran Surulivel , MSPAND Technologies Pvt Ltd
Mr.Suprovab Mandal , Microchip , Malaysia.
Dr.Sivanantham , Professor & Dean,VIT.
Dr.R.Sakthivel , Professor,VIT.
Dr.JagannadhaNaidu, HOD-MNE, VIT.
Dr.Ravi S, Asso. Professor, VIT.

Guidelines

The FDP will be conducted in Physical Mode.

There will be 12 sessions in six days and two sessions every day. And one session may be utilized for feedback and assessment.

As per AICTE Training and Learning (ATAL) Academy guidelines no registration fee will be charged from the participants.

80 % Attendance is mandatory for claims.

Resource Persons

Resource persons are from various IIT's, NIT's, State & Central Universities and Industries.

Eligibility

This AICTE sponsored FDP is open to the faculty members of AICTE approved Institutions, Research scholars, participants from Government, Industry (Bureaucrats/Technicians/Participants from Industry etc.) and staff of host institutions.

Key dates

Last Date for Application: 20.11..2023

Date of the FDP: 11.12.2023 to 16.12.2023

For Further details

Coordinators

FDP- (Si2CHIP-23),
Dr.Ravi S
Dr.Sakthivel Ramachandran

E-mail : msravi@vit.ac.in ;
rsakthivel@vit.ac.in

Mobile : 9790155650,
9994627570

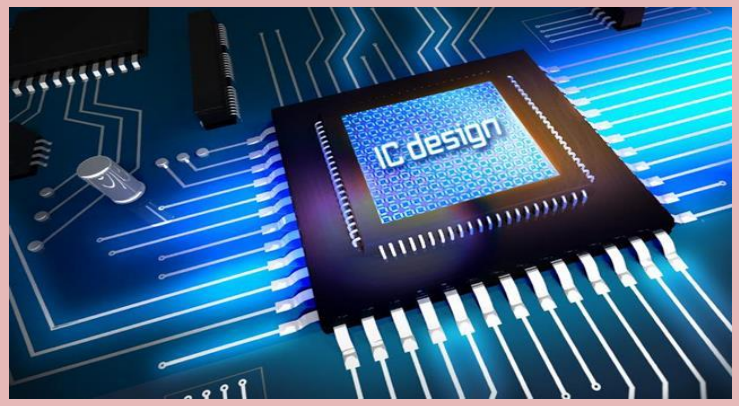
Follow us on

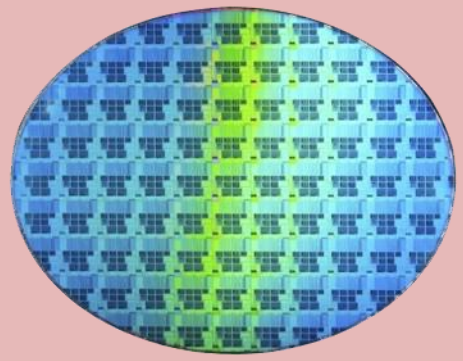
https://www.linkedin.com/events/7112327477707886594/comments/

"ATAL AICTE Sponsored SIX Days Faculty Development Program on
"Silicon to Chip Design"
11th to 16th Dec 2023
Application Number : 1691730133
Dept. of Micro and Nanoelectronics, SENSE , VIT, Vellore.

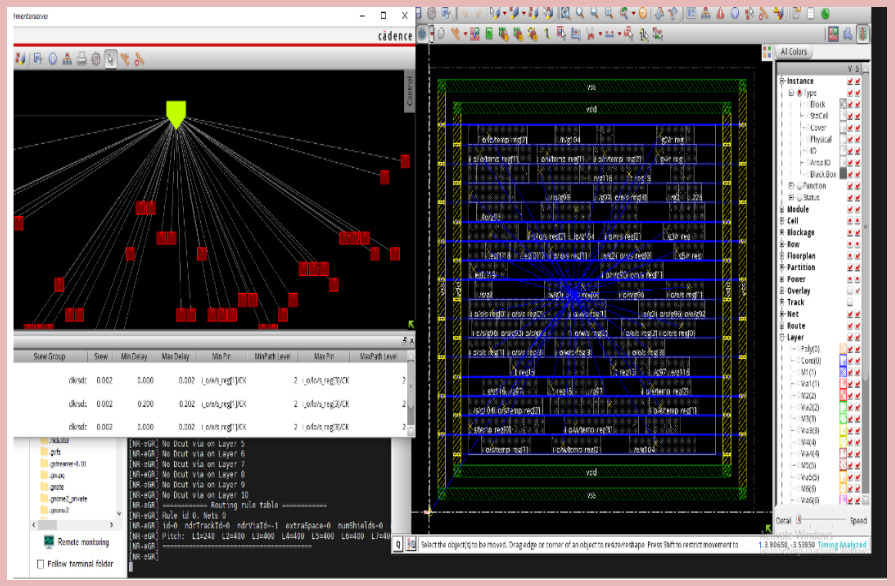
VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

Tape out - Chip





- DRC / LVS
- Routing
- CTS
- Placement
- Power Plan
- Floor Plan
- Physical Aware Synthesis
- Synthesis
- Simulation
- &
- RTL Design
- Silicon



Coordinators
Dr. Ravi S -9790155650 :
msravi@vit.ac.in
Dr. Sakthivel R -9994627570
rsakthivel@vit.ac.in

Important instruction
No Registration Fee
TA/DA Will be provided as per the AICTE norms
For Registration
https://atalacademy.aicte-india.org/login

Faculty / PG/TRA / JRF/SRF Only

ATAL
Registration ID : 1691730133