VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

tttc

TTTC Seminar on

VLSI Testing and Testability

March 13-15, 2020

Venue:

Department of Micro and Nano Electronics

School of Electronics Engineering

Vellore Institute of Technology,

Vellore, Tamil Nadu– 632 014

For registration, please visit:

https://events.vit.ac.in/

Speakers

Professionals from various Semiconductor Industries sponsored by

Test Technology Technical Council (India)

(https://site.ieee.org/tttc-india/)

&

Faculty members from

Vellore Institute of Technology, Vellore

(https://vit.ac.in)

TOPICS

DAY 1 (13/03/2020)

DFX as a Career: Choice or Compromise

- Myths and Facts
- Impact, Complexity and Challenges
- DFX as Functional Feature with Paradigm Shift in Semiconductor Market

Evolution of Design for Test – Part 1

- Limitation of Functional Testing and Need for Defect Oriented Testing
- Defect Mechanisms and Fault Models
- Overview of Automatic Test Equipment
- Silicon Bring up: Debug flow/Shmoo plot analysis
- Manufacturing process: (Wafer Sort -> Final Test -> System Level Test, test cost at different levels)
- Legacy Scan based Testing
- Fault Models: Stuck and Transition delay
- Slack measurement – GBA & PBA
- Transition Fault Testing: LoC and LoS
  - Respective Advantages and Disadvantages of LoC and LoS
  - Transition Fault Testing Across Clock Domains
- Scan Compression: Need for Scan Compression, Combinatorial Scan Compression (Adaptive Scan), Sequential Scan Compression (EDT/OPMISR/DFT Max Ultra), Impact of X on Scan Compression and X handling, Aliasing

Evolution of Design for Test – Part 2

- Logic BIST
- IEEE 1149.1 JTAG
  - Need for JTAG
  - TAP Controller Architecture
  - TAP Controller FSM

DAY 2 (14/03/2020)

Memory Testing

- Fault Models
- Test Algorithms
- MBIST Controller Architecture and Diagnosis
- Memory repair

High-speed IO Testing

- High Speed I/O Testing: Challenges, Loopback Test, Characterization
- High-speed Serial I/O
- Test Planning for Complex SOC

Advanced Fault models

- Motivation
- New Defect Mechanisms (FinFET)
- Traditional Scan Test: Defect Escapes
- Cell Aware Test
- Small Delay Defect Testing
- Challenges and Mitigation

Test Diagnosis

- Scan Diagnosis: Diagnosis methodology for Scan based designs ,Methods & Best practices, Diagnostic resolution, Debugging
- Logic BIST diagnosis

DAY 3 (15/03/2020)

Hand-on Lab Sessions on Tessent DFT Tools from Mentor Graphics

- Scan Insertion and DRC Analysis
- Scan Compression Logic Insertion
- Boundary Scan (JTAG 1149.1) Implementation
- Automatic Test Pattern (ATPG) Generation
- ATPG Pattern Simulation

Supported by

Mentor
A Siemens Business

Who can apply?

- Faculty members & Research Scholars
- DFT Professionals
- Students from M.E./M.Tech (VLSI Design / Applied Electronics), B.E./B.Tech. (ECE/EEE), Research Scholars Students

Prerequisite

Basic knowledge on Digital Logic Design and VLSI Design Flow

Registration Fee *(inclusive of 18% GST)*

UG/PG Students	Rs. 700/-
Faculty Members / Research Scholars	Rs. 1000/-
Industry Professional	Rs.1500/-

**Registration fee includes seminar kit, working lunch and refreshments only. Accommodation will be provided based on availability in Student's Hostel with extra charges.*

For registration and payment of registration fee:

https://events.vit.ac.in/

Last date for registration: 11/03/2020 (Wednesday)

For more details please contact:

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