VIT®
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

Five Day
Faculty Development Program on

VLSI TECHNIQUES FOR DSP SYSTEM DESIGN USING FPGAS

December 07 - 11, 2022

About VIT

VIT was established to provide quality higher education on par with international standards. It persistently seeks and adopts innovative methods to improve the quality of higher education consistently. The campus has a cosmopolitan atmosphere with students from all corners of the globe. Experienced and learned teachers are strongly encouraged to nurture the students. The global standards set at VIT in the field of teaching and research spur us on in our relentless pursuit of excellence. It has become a way of life for us. The highly motivated youngsters on the campus are a constant source of pride. Our Memoranda of Understanding with various international universities are our major strength. They provide for an exchange of students and faculty and encourage joint research projects for the mutual benefit of these universities. Many of our students, who pursue their research projects in foreign universities, bring high quality to their work and esteem to India and have done us proud. VIT has ranked in the top 251-300 in THE world University rankings. VIT has been ranked 12th in Research, 12th in Engineering Category, 13th in University Category and 21st in Overall Category by the MHRD-NIRF Ranking. It is given the status of institute of eminence by the Govt of INDIA. VIT University obtained the highest possible grade of "A++" from NAAC during the re-accreditation process. With steady steps, we continue our march forward. We look forward to meeting you here at VIT.

About School of Electronics Engineering (SENSE)

SENSE at VIT was established for imparting state-of-the-art knowledge in Electronics and Communication Engineering and allied areas. B.Tech. Electronics and Communication Engineering is accredited by the Engineering Accreditation Commission of ABET. Eligible students are placed on campus and many of them are placed in core companies every year. The school has set up laboratories with excellent infrastructure in the areas of Electronics, Communication, VLSI, Embedded, and Sensors. The latest simulation tools are used to cater to various specializations and are equipped with facilities for measurement, characterization, and synthesis of experimental as well as theoretical results. Students are encouraged to take up their final year projects abroad too. The school has many industry-sponsored advanced laboratories for carrying out research and development. MoUs with many Foreign Universities, Research Organizations, and Industries facilitate student and faculty exchange. Faculty are actively involved in R&D activities and are working on research projects funded by government organizations like DRDO, ISRO, and agencies like DST.

About FDP

The digital signal processing (DSP) applications are in numerous infotainments, medical diagnostics and advanced communication and radar systems. Always the advancement in VLSI technologies will have an impact on the performance of these systems. With the non-terminating nature of the DSP systems, even a small performance improvement in the implementation of an arithmetic functional unit will have a greater impact on the whole system. VLSI DSP deals with such architectural and algorithmic optimization techniques to design high-performance DSP systems. As VLSI DSP needs inter-domain expertise of both DSP and VLSI domains, there is a huge necessity to impart the necessary concepts and hands-on skills to research scholars and faculty.

This FDP intends to fill the gap by providing not only theoretical knowledge on DSP architectural transformation and numerical strength reductions and also intends to the following:

1. MATLAB for DSP VLSI system design
2. Hands-on training on INTEL FPGAs
3. A demo and hands-on using DSP builder
4. Design practice and trends in major industries

Target Participants

Faculty, Research scholars and budding engineers who are working in the industry

Course Contents

Day 1
Introduction to DSP VLSI
Architectural transformation techniques (Retiming, Folding)
Day 2
Architectural transformation techniques (Unfolding)
Numerical strength reduction techniques
Hands-on MATLAB for VLSI DSP
Day 3
Numerical strength reduction techniques
Introduction to INTEL FPGA Design flow
Hands-on: Implementation using INTEL FPGAs
Day 4
Introduction to DSP builder
Design flow using DSP Builder
Hands-on: Implementation using DSP Builder
Day 5
Industry practice and trends in DSP VLSI system design

Resource Persons

1. Dr. V. Arunachalam, Asso. Prof, SENSE
2. Dr . K.Sivasankaran, Asso. Prof, SENSE
3. Dr. Sri Adibhatla Sridevi, Asso. Prof., SENSE
4. Dr. P Jayakrishnan, Asst .Prof, SENSE
5. Mr Padmanabhan, Intel PSG, India

Registration Fees

- Industry Participants : Rs 4130/-*
- Faculty/Student / Research Scholar (External / Internal) : Rs 3540/-*
- Active IEEE Members during the year 2022 (Internal & External) : Rs 2950/-*

(* - Inclusive of 18% GST)

(Registration fee Includes a kit with a book titled VLSI DSP systems authored by Keshab K Parhi, working lunch and refreshments. A certificate will be issued to all the registered participants.)

Payment link

The registration fee has to be paid through the following payment link only.

https://events.vit.ac.in/

Important Dates:

Last date for registration: October 5, 2022

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