VIT®

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

Vellore, Tamil Nadu – 632014

Three day National TTTC Workshop

On

VLSI Test and Reliability

7th to 9th April 2023

Organized by

School of Electronics Engineering

In association with

Test Technology Technical Community

(TTC India)

Venue: Gallery II, Technology Tower,

VIT, Vellore

Time: 9.30 a.m. – 6.00 p.m.

For registration, please visit:

https://events.vit.ac.in/

About VIT

VIT was established with the aim of providing quality higher education on par with international standards. It persistently seeks and adopts innovative methods to improve the quality of higher education on a consistent basis.The campus has a cosmopolitan atmosphere with students from all corners of the globe. Experienced and learned teachers are strongly encouraged to nurture the students. The global standards set at VIT in the field of teaching and research spur us on in our relentless pursuit of excellence. Our Memoranda of Understanding with various international universities are our major strength. They provide for an exchange of students and faculty and encourage joint research projects for the mutual benefit of these universities. With steady steps, we continue our march forward. We look forward to meeting you here at VIT.

About School of Electronics Engineering

SENSE at VIT was established for imparting state-of-the-art knowledge in Electronics and Communication Engineering and allied areas. The school has set up laboratories with excellent infrastructure in the areas of Electronics, Communication, VLSI, Embedded, Sensors and Nanotechnology. The latest simulation tools are used to cater to various specializations and are equipped with facilities for measurement, characterization and synthesis of experimental as well as theoretical results. The School has many industry sponsored advanced laboratories for carrying research and development. MoUs with many Foreign Universities, Research Organizations and Industries facilitate student and faculty exchange.

About TTTC

IEEE Test Technology Technical Community (TTTC) is a very reputed council being run by IEEE Computer Society working in the domain of VLSI Design and Test. The industry veterans of the VLSI testing field who are the major volunteers of TTTC are contributing for this workshop.

About Workshop

The program is intended for the Faculty, UG and PG students, research scholars, practicing engineers and people from R & D in the field of VLSI Design. The main objective of the program is to provide the concepts Design for Testing, Scan based Testing, Scan Compression, Test Standards, Memory Testing, Test Diagnosis, Advanced Fault Modeling and Hands on sessions using Tessent DFT Tools from Siemens EDA (Mentor) tools. You will earn a digital bagde from Siemens EDA on successful completion of this program.

Who can apply?

- **Faculty members & Research Scholars**
- **DFT Professionals**
- **Students from M.E./M.Tech (VLSI Design / Applied Electronics), B.E./B.Tech. (ECE/EEE), Research Scholars Students**

Prerequisite:

Basic knowledge on Digital Logic Design and VLSI Design Flow

Registration Fees

Participant Type	Amount (Inclusive 18% GST)
UG / PG Student	Rs. 750/-
Faculty / Research Scholars	Rs. 1000/-

Registration fee includes a kit, working lunch and refreshments only. Participants are requested to make their own arrangements for accommodation if possible. Limited number participants can be provided accommodation based on availability in students hostel on paid basis (Dormitory in Men's hostel, 4 bedded Non AC and AC rooms in ladies hostel). Certificate will be issued to all the participants.

Registration & Payment Link:

https://events.vit.ac.in/

Applications will be accepted on a first come first serve basis. Number of participants is limited to 100.

Last Date for Registration: 1st April 2023.

Topics

DFX as a Career: Choice or Compromise

- Myths and Facts
- Impact, Complexity and Challenges
- DFX as Functional Feature with Paradigm Shift in Semiconductor Market

Evolution of Design for Test – Part 1

- Limitation of Functional Testing and Need for Defect Oriented Testing
- Defect Mechanisms and Fault Models
- Overview of Automatic Test Equipment
- Silicon Bring up:
- Debug flow/Shmoo plot analysis
- Manufacturing process:
- (Wafer Sort -> Final Test -> System Level Test, test cost at different levels)
- Legacy Scan based Testing
- Fault Models: Stuck and Transition delay
- Slack measurement – GBA & PBA
- Transition Fault Testing: LoC and LoS
- Respective Advantages and Disadvantages of LoC and LoS
- Transition Fault Testing Across Clock Domains
- Scan Compression: Need for Scan Compression, Combinatorial Scan Compression (Adaptive Scan), Sequential Scan Compression (EDT/OPMISR/DFT Max Ultra), Impact of X on Scan Compression and X handling, Aliasing

Evolution of Design for Test – Part 2

- Logic BIST
- IEEE 1149.1 JTAG
- Need for JTAG
- TAP Controller Architecture
- TAP Controller FSM

Memory Testing

- Fault Models
- Test Algorithms
- MBIST Controller Architecture and Diagnosis
- Memory repair

Advanced Fault models

- Island Motivation
- New Defect Mechanisms (FinFET)
- Traditional Scan Test: Defect Escapes
- Cell Aware Test
- Small Delay Defect Testing
- Challenges and Mitigation

Test Diagnosis

- Scan Diagnosis: Diagnosis methodology for Scan based designs, Methods & Best practices, Diagnostic resolution, Debugging
- Logic BIST diagnosis

Hand-on Lab Sessions on Tessent DFT Tools from Siemens EDA Mentor Graphics

- Scan Insertion and DRC Analysis
- Scan Compression Logic Insertion
- Automatic Test Pattern (ATPG) Generation
- ATPG Pattern Simulation
- Scan Compression
- Memory BIST

SIEMENS Mentor A Siemens Business

Speakers

NAVIN BISHNOI
Country Head, Marvell Semiconductors

PRASAD MANTRI
Chief Technical officer,AISemiCon

ABISHEK CHOUDHARY
Digital Design Makers,Texas Instruments

LEELA KRISHNA
Texas Instruments Senior Engineer II,
Synopsys India

SARTHAK SINGHAL
Candence Design System

RENOLD SAM
Silicon Design Engineering, AMD

Prof. USHA MEHTA
HoD, ECE
Nirma University, Ahemdabad

Prof. SIVANANTHAM S
Dean, SENSE
VIT Vellore

Advisory Committee

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Advisors

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