VIT®

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

School of Electronics Engineering (SENSE)

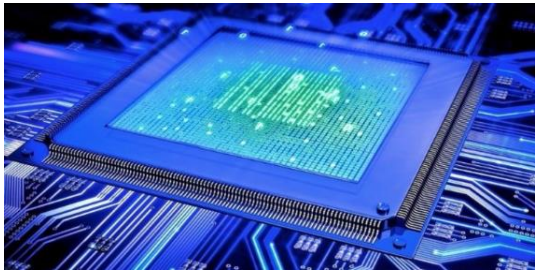
Department of Micro & Nano Electronics

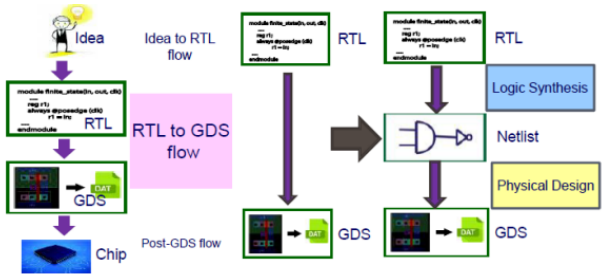
Offers

Value Added Programme

on

RTL to GDSII





25-26 March & 1st April, 2023

About Training:

With today's increasingly large and complex digital IC and system-on-chip (SoC) designs, design power closure, circuit power integrity and Testing become one of the main engineering challenges, thereby impacting the device's total time-to-market. This Training will teach you how to implement a design from RTL-to-GDSII using various industry standard tools. You will start by coding a design in Verilog, simulate, synthesize and optimize for a better design.

Who Can Attend?

➔ VIT Students –UG/PG .

Key Benefits:

This course is designed to introduce the engineers to the area of specification to chip design. The candidates who successfully undergo this training would be able to design a digital system optimized in terms of area, power and timing by applying appropriate constraints. It enable them to apply all possible Power minimization and DFT techniques to build a more reliable system. It provides them the usage of industry Tool knowledge right from specification to GDSII.

Last date for Registration:

On or before : 22nd March 2023

Course Fee:

Registration Fee: VIT Student: **Rs.500/-**
(Inclusive of GST)

Certificate, Course Material will be provided.

Course Content:

- FSM Coding Guideline and Coding Style for Synthesis
- Architecture of Logic Synthesizer
- Synthesis Optimization- Timing Parameter Definition – Setup and Hold Timing Check
- Multicycle Paths- Half-Cycle Paths- False Paths.
- Low Power Synthesis
- DFT Based Synthesis.
- Pattern Generation- Fault Simulation – Scan Chain Insertion- Fault Coverage.
- Floor plan, Placement, CTS and routing– ECO flow – Signal Integrity Issues,
- Timing Sign-off, Physical Verification.

Convener:

Prof. S. Sivanantham
Dean, School of Electronics (SENSE)

Co-Convener:

Prof. Jagannadha Naidu K
HoD, Department of Micro & Nano Electronics

Coordinators:

➔ **Dr. Sakthivel R**
Professor

➔ **Dr. Jagannadha Naidu K,**
Assistant Professor (Senior)

For Registration contact:

Mr.V.Karthikeyan
Contact No.: 9894972399

Registration Venue:

Technology Tower: TT237

Event Venue:

TT238, Technology Tower

Online Payment link

Link: https://events.vit.ac.in/