



28<sup>TH</sup> IEEE INTERNATIONAL SYMPOSIUM ON VLSI DESIGN AND TEST

**VDAT 2024** 

VIT Vellore, Tamil Nadu, India

School Of Electronics Engineering (SENSE)

**Presents** 

# HANDS ON VLSI DESIGN

**USING CADENCE TOOLS** 

Pre-VDAT workshop

10<sup>th</sup> - 11<sup>th</sup>August, 2024

237A, Technology Tower

REGISTER AT: https://events.vit.ac.in/

cadence

### **About VDAT**

The VLSI Design & Test Symposium (VDAT) began as a workshop in 1998 and became a symposium in 2005 due to growing participation. Since then, VDAT has been held annually, becoming a key event for VLSI professionals and academics. The symposium offers opportunities for academia, researchers, startups, and industry practitioners to share ideas, experiences, and knowledge in VLSI Design and Testing.

Over 27 years, this annual event has introduced many novel designs and technologies, contributing to global advancements in VLSI. High-quality technical paper presentations have guided participants towards new directions in VLSI technology.

In its 28th year, VDAT-2024 will be a three-day inperson event at the Vellore Institute of Technology (VIT), Vellore, Tamil Nadu, from O September 1-3, 2024. VDAT-2024 is supported by the VLSI Society of India.

## Who Can Attend?

All VIT Undergraduate Students

**Last Date for Registration** 

9<sup>th</sup> August 2024

**Event Fee** 

₹ 250 only

**CERTIFICATES** will be provided

## **Course Content**

- RTL Design: Introduction to Register Transfer Level (RTL) design
- RTL Simulation: Verifying the functionality of RTL code with Cadence simulation tools
- Gate Level Simulation: Simulating postsynthesis netlist to ensure design correctness
- Synthesis: Converting RTL code into a gate-level netlist using synthesis tools
- Physical design: Translating gate-level netlist into a physical layout with placement and routing

#### Convener:

Dr. S. Sivanantham Dean, School of Electronics Engineering (SENSE)

#### Co-Convener:

Dr. Jagannadha Naidu K HoD, Department of Micro & Nano Electronics

### **Coordinators:**

Dr. S. Ravi, Associate Professor Dr. Rajeev Pankaj, Associate Professor

For Registration contact:

Bhavesh Sai

Contact No.: 7989269410

Required software will be provided