VIT®

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

SCHOOL OF ELECTRONICS ENGINEERING

M. Tech VLSI Design

(M.Tech MVD)

Curriculum

(*2021-2022 admitted students*)

VISION STATEMENT OF VELLORE INSTITUTE OF TECHNOLOGY

Transforming life through excellence in education and research.

MISSION STATEMENT OF VELLORE INSTITUTE OF TECHNOLOGY

World class Education: Excellence in education, grounded in ethics andcritical thinking, for improvement of life.

Cutting edge Research: An innovation ecosystem to extend knowledge andsolve critical problems.

Impactful People: Happy, accountable, caring and effective workforce andstudents.

Rewarding Co-creations: Active collaboration with national & internationalindustries & universities for productivity and economic development.

Service to Society: Service to the region and world through knowledge andcompassion.

VISION STATEMENT OF THE SCHOOL OF ELECTRONICS ENGINEERING

To be a leader by imparting in-depth knowledge in Electronics Engineering, nurturing engineers, technologists and researchers of highest competence, who would engage in sustainable development to cater the global needs of industry and society.

MISSION STATEMENT OF THE SCHOOL OF ELECTRONICS ENGINEERING

- Create and maintain an environment to excel in teaching, learning and applied research in the fields of electronics, communication engineering and allied disciplines which pioneer for sustainable growth.
- Equip our students with necessary knowledge and skills which enable them to be lifelong learners to solve practical problems and to improve the quality of human life.

M. Tech. VLSI Design

PROGRAMME EDUCATIONAL OBJECTIVES (PEOs)

1. Graduates will be engineering practitioners and leaders, who would help solve industry's technological problems.

2. Graduates will be engineering professionals, innovators or entrepreneurs engaged in technology development, technology deployment, or engineering system implementation in industry.

3. Graduates will function in their profession with social awareness and responsibility.

4. Graduates will interact with their peers in other disciplines in industry and society and contribute to the economic growth of the country.

5. Graduates will be successful in pursuing higher studies in engineering or management.

6. Graduates will pursue career paths in teaching or research.

M. Tech VLSI Design

PROGRAMME OUTCOMES (POs)

PO_01: Having an ability to apply mathematics and science in engineering applications.

PO_02: Having an ability to design a component or a product applying all the relevant standards and with realistic constraints, including public health, safety, culture, society and environment

PO_03: Having an ability to design and conduct experiments, as well as to analyse and interpret data, and synthesis of information

PO_04: Having an ability to use techniques, skills, resources and modern engineering and IT tools necessary for engineering practice

PO_05: Having problem solving ability- to assess social issues (societal, health, safety, legal and cultural) and engineering problems

PO_06: Having adaptive thinking and adaptability in relation to environmental context and sustainable development

PO_07: Having a clear understanding of professional and ethical

responsibility

PO_08: Having a good cognitive load management skills related to project management and finance

PROGRAMME SPECIFIC OUTCOMES (PSOs)

On completion of M. Tech. (VLSI Design) programme,
graduates will be able to

PSO1: Apply advanced concepts in Physics of semiconductor devices to design VLSI Systems.

PSO2: Design ASIC and FPGA based systems using industry standard tools.

PSO3: Solve research gaps and provide solutions to socio-economic, and environmental problems.

Category-wise Credit distribution

Category	Credits
University core (UC)	**27**
Programme core (PC)	**19**
Programme elective (PE)	**18**
University elective (UE)	**6**
Bridge course (BC)	
Total credits	**70**

Detailed curriculum

(as given in the student curriculum view – in the order of UC, UE, PC and PE). Courses need not be listed under UE.

University Core - 27 Credits

S. No	Course Code	Course Title	L	T	P	J	C
1.	MAT5009	Advanced Computer Arithmetic	2	2	0	0	3
2.	ENG5001 and ENG5002 (or) EFL5097	Technical English I and Technical English II (or) Foreign Language	{0 0 2	0 0 0	2 2 0	0 0} 0	2
3.	STS5001	Soft Skills	0	0	0	0	1
4.	STS5002	Soft Skills	0	0	0	0	1
5.	SET5001	SET Project-I	0	0	0	0	2
6.	SET5002	SET Project-II	0	0	0	0	2
7.	ECE6099	Master's Thesis	0	0	0	0	16

University Elective – 6 Credits

S.No		Course Title	L	T	P	J	C
1		University Elective[#]	-	-	-	-	6

 # All courses offered by other M.Tech Programmes / PE of M.Tech (VLSI Design)

Programme Core – 19 Credits

S. No	Course Code	Course Title	L	T	P	J	C
1	**ECE5014**	ASIC Design	3	0	2	0	4
2	**ECE5015**	Digital IC Design	3	0	0	4	4
3	**ECE5016**	Analog IC Design	3	0	2	0	4
4	**ECE5017**	Digital Design with FPGA	2	0	2	4	4
5	**ECE5018**	Physics of VLSI Devices	3	0	0	0	3

Programme Electives - 18 Credits

S. No	Course Code	Course Title	L	T	P	J	C
1	**ECE5019**	Computer Aided Design for VLSI	3	0	0	0	3
2	**ECE5020**	DSP Architectures	2	0	0	4	3
3	**ECE5022**	VLSI Digital Signal Processing	3	0	0	0	3
4	**ECE5023**	Memory Design and Testing	3	0	0	0	3
5	**ECE5024**	IC Technology	3	0	0	0	3
6	**ECE5025**	System-on-Chip Design	3	0	0	0	3
7	**ECE5026**	System Design with FPGA	2	0	0	4	3
8	**ECE5027**	Advanced Computer Architecture	3	0	0	0	3
9	**ECE5028**	Micro Sensors and Interface Electronics	2	0	0	4	3
10	**ECE5029**	VLSI Testing and Testability	3	0	0	0	3
11	**ECE5030**	Scripting languages for VLSI design automation	2	0	2	0	3
12	**ECE6024**	VLSI Verification Methodologies	2	0	0	4	3
13	**ECE6025**	Low Power IC Design	2	0	0	4	3
14	**ECE6026**	Mixed Signal IC Design	2	0	0	4	3
15	**ECE6027**	RFIC Design	2	0	0	4	3
16	**ECE6028**	Nanoscale Devices and Circuit Design	2	0	0	4	3

Syllabus

Course Code	Course Title	L	T	P	J	C
MAT5009	ADVANCED COMPUTER ARITHMETIC	2	2	0	0	3
Pre-requisite	None					Syllabus version

Course Objectives:

The course aimed to:

1. Introduce the representation of the numbers using redundant and residue number system.
2. Introduce various integer arithmetic algorithms, FFT and modular arithmetic algorithms.
3. Familiarize floating-point arithmetic algorithms and its impacts on resulting error and its corrective methods.
4. Explain CORDIC algorithm for calculating various functions of common interest.
5. Explains the implementation aspects of high throughput, low power and fault tolerant arithmetic circuits.

Expected Course Outcome:

The students will be able to:

1. Understand and represent the numbers using redundant and residue number system.
2. Understand and apply various integer arithmetic algorithms.
3. Understand and apply various FFT and modular arithmetic algorithms.
4. Understand floating-point arithmetic algorithms, apply it, analyse the impacts of resulting error and its corrective methods.
5. Understand and apply CORDIC algorithm for calculating various functions of common interest.
6. Understand the implementation aspects of high throughput, low power and fault tolerant arithmetic circuits.

Module:1	Introduction to computer Arithmetic	5 hours

Review of Numbers and arithmetic. Redundant number systems. Residue number system.

Module:2	Integer Arithmetic	7 hours

Addition and Subtraction. Multiplication. Division. Roots. Greatest Common Division. Base Conversion: Quadratic Algorithms, Sub quadratic Algorithms.

Module:3	FFT and Modular Arithmetic	6 hours

Representation: Classical Representation, Montgomery's Form, Residue Number Systems, MSB vs LSB Algorithms, Link with Polynomials. Addition and Subtration. Multiplication: Barrett's Algorithm, Montgomery's Multiplication, McLaughlin's Algorithm, Special Moduli, Fast Multiplication Over GF (2)[x]. Division and Inversion, Exponentiation, Chinese Remainder Theorem.

Module:4	Floating Point Arithmetic	7 hours

Floating point representation. Floating point operation. Errors and Error control. Precise and certifiable arithmetic.

Module:5	Function Evaluation	7 hours

Square-Rooting Methods. The CORDIC Algorithms . Variations in Function Evaluation. Arithmetic by Table Lookup.

Module:6	Implementations	5 hours

High throughput arithmetic, Low power arithmetic, fault tolerant arithmetic			
Module:7	**Error Analysis**		**6 hours**
Absolute Versus Relative Error, Significant Digits. Uncertainty in Data. Chopping off and Rounding off. Truncation Error. Loss of Significance.			
Module:8	**Contemporary issues:**		**2 hours**
	Total Lecture hours:		**45 hours**
Text Books			
1.	Behrooz Parhami, "Computer Arithmetic: Algorithms and Hardware Design", (2/e) Oxford University Press 2015.		
2.	Richard P Brent and Paul Zimmerman, "Modern Computer Arithmetic", Cambridge University Press 2010.		
Reference Books			
1.	Mircea Vladutiu, "Computer Arithmetic: Algorithms and Hardware Implementation", Springer 2012.		
2.	Ulrich W. Kulisch "Computer Arithmetic and Validity: Theory, Implementation, and Applications", De Gruyter; 2 edition, 2012		
Mode of Evaluation: Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).			
Recommended by Board of Studies	17-02-2016		
Approved by Academic Council	No. 47	Date	05-10-2017

Course code	Course title	L	T	P	J	C
ENG5001	Fundamentals of Communication Skills	0	0	2	0	1
Pre-requisite	Not cleared EPT (English Proficiency Test)					Syllabus version
						1.0

Course Objectives:

1. To enable learners learn basic communication skills - Listening, Speaking, Reading and Writing
2. To help learners apply effective communication in social and academic context
3. To make students comprehend complex English language through listening and reading

Expected Course Outcome:

1. Enhance the listening and comprehending skills of the learners
2. Acquire speaking skills to express their thoughts freely and fluently
3. Learn strategies for effective reading
4. Write grammatical correct sentences in general and academic writing
5. Develop technical writing skills like writing instructions, transcoding etc.,

Module:1	Listening	**8 hours**
Understanding Conversation Listening to Speeches Listening for Specific Information		
Module:2	Speaking	**4 hours**
Exchanging Information Describing Activities, Events and Quantity		
Module:3	Reading	**6 hours**
Identifying Information Inferring Meaning Interpreting text		
Module:4	Writing: Sentence	**8hours**
Basic Sentence Structure Connectives Transformation of Sentences Synthesis of Sentences		
Module:5	Writing: Discourse	**4hours**
Instructions Paragraph Transcoding		
	Total Lecture hours:	**30 hours**

Text Book(s)

1. Redston, Chris, Theresa Clementson, and Gillie Cunningham. Face2face Upper Intermediate Student's Book. 2013, Cambridge University Press.

Reference Books

1. Chris Juzwiak .Stepping Stones: A guided approach to writing sentences and Paragraphs (Second Edition), 2012, Library of Congress.
2. Clifford A Whitcomb & Leslie E Whitcomb, Effective Interpersonal and Team

3. 4. 5. 6.	Communication Skills for Engineers, 2013, John Wiley & Sons, Inc., Hoboken: New Jersey. ArunPatil, Henk Eijkman &Ena Bhattacharya, New Media Communication Skills for Engineers and IT Professionals,2012, IGI Global, Hershey PA. Judi Brownell, Listening: Attitudes, Principles and Skills, 2016, 5th Edition, Routledge:USA John Langan, Ten Steps to Improving College Reading Skills, 2014, 6th Edition, Townsend Press:USA Redston, Chris, Theresa Clementson, and Gillie Cunningham. Face2face Upper Intermediate Teacher's Book. 2013, Cambridge University Press.
	Authors, book title, year of publication, edition number, press, place

Mode of Evaluation: CAT / Assignment / Quiz / FAT / Project / Seminar

List of Challenging Experiments (Indicative)		
1.	Familiarizing students to adjectives through brainstorming adjectives with all letters of the English alphabet and asking them to add an adjective that starts with the first letter of their name as a prefix.	2 hours
2.	Making students identify their peer who lack Pace, Clarity and Volume during presentation and respond using Symbols.	4 hours
3.	Using Picture as a tool to enhance learners speaking and writing skills	2 hours
4.	Using Music and Songs as tools to enhance pronunciation in the target language / Activities through VIT Community Radio	2 hours
5.	Making students upload their Self- introduction videos in Vimeo.com	4 hours
6.	Brainstorming idiomatic expressions and making them use those in to their writings and day to day conversation	4 hours
7.	Making students Narrate events by adding more descriptive adjectives and add flavor to their language / Activities through VIT Community Radio	4 hours
8	Identifying the root cause of stage fear in learners and providing remedies to make their presentation better	4 hours
9	Identifying common Spelling & Sentence errors in Letter Writing and other day to day conversations	2 hours
10.	Discussing FAQ's in interviews with answers so that the learner gets a better insight in to interviews / Activities through VIT Community Radio	2 hours
	Total Practical Hours	30 hours

Mode of evaluation: Online Quizzes, Presentation, Role play, Group Discussions, Assignments, Mini Project

Recommended by Board of Studies	22-07-2017		
Approved by Academic Council	No. 46	Date	24-8-2017

Course Code	Course Title	L	T	P	J	C
ENG5002	Professional and Communication Skills	0	0	2	0	1
Pre-requisite	ENG5001					Syllabus version
						1.1

Course Objectives:

1. To enable students to develop effective Language and Communication Skills
2. To enhance students' Personal and Professional skills
3. To equip the students to create an active digital footprint

Expected Course Outcome:

1. Improve inter-personal communication skills
2. Develop problem solving and negotiation skills
3. Learn the styles and mechanics of writing research reports
4. Cultivate better public speaking and presentation skills
5. Apply the acquired skills and excel in a professional environment

Module:1	Personal Interaction	2hours

Introducing Oneself- one's career goals

Activity: SWOT Analysis

Module:2	Interpersonal Interaction	2 hours

Interpersonal Communication with the team leader and colleagues at the workplace

Activity: Role Plays/Mime/Skit

Module:3	Social Interaction	2 hours

Use of Social Media, Social Networking, gender challenges
Activity: Creating LinkedIn profile, blogs

Module:4	Résumé Writing	4 hours

Identifying job requirement and key skills
Activity: Prepare an Electronic Résumé

Module:5	Interview Skills	4 hours

Placement/Job Interview, Group Discussions
Activity: Mock Interview and mock group discussion

Module:6	Report Writing	4 hours

Language and Mechanics of Writing

Activity: Writing a Report

Module:7	Study Skills: Note making	2hours

Summarizing the report
Activity: Abstract, Executive Summary, Synopsis

Module:8	**Interpreting skills**	**2 hours**
Interpret data in tables and graphs Activity: Transcoding		
Module:9	**Presentation Skills**	**4 hours**
Oral Presentation using Digital Tools Activity: Oral presentation on the given topic using appropriate non-verbal cues		
Module:10	**Problem Solving Skills**	**4 hours**
Problem Solving & Conflict Resolution Activity: Case Analysis of a Challenging Scenario		
	Total Lecture hours:	**30hours**

Text Book(s)

	Bhatnagar Nitin and Mamta Bhatnagar, Communicative English For Engineers And Professionals, 2010, Dorling Kindersley (India) Pvt. Ltd.	

Reference Books

	Jon Kirkman and Christopher Turk, Effective Writing: Improving Scientific, Technical and Business Communication, 2015, Routledge Diana Bairaktarova and Michele Eodice, Creative Ways of Knowing in Engineering, 2017, Springer International Publishing Clifford A Whitcomb & Leslie E Whitcomb, Effective Interpersonal and Team Communication Skills for Engineers, 2013, John Wiley & Sons, Inc., Hoboken: New Jersey. ArunPatil, Henk Eijkman &Ena Bhattacharya, New Media Communication Skills for Engineers and IT Professionals,2012, IGI Global, Hershey PA.

Mode of Evaluation: CAT / Assignment / Quiz / FAT / Project / Seminar

List of Challenging Experiments (Indicative)

1.	SWOT Analysis – Focus specially on describing two strengths and two weaknesses	2 hours
2.	Role Plays/Mime/Skit -- Workplace Situations	4 hours
3.	Use of Social Media – Create a LinkedIn Profile and also write a page or two on areas of interest	2 hours
4.	Prepare an Electronic Résumé and upload the same in vimeo	2 hours
5.	Group discussion on latest topics	4 hours
6	Report Writing – Real-time reports	2 hours
7	Writing an Abstract, Executive Summary on short scientific or research articles	4 hours
8	Transcoding – Interpret the given graph, chart or diagram	2 hours

9	Oral presentation on the given topic using appropriate non-verbal cues	4 hours
10	Problem Solving -- Case Analysis of a Challenging Scenario	4 hours
	Total Laboratory Hours	30 hours

Mode of evaluation: : Online Quizzes, Presentation, Role play, Group Discussions, Assignments, Mini Project			
Recommended by Board of Studies	22-07-2017		
Approved by Academic Council	No. 47	Date	05-10-2017

Course Code	Course Title	L	T	P	J	C
GER5001	Deutsch für Anfänger	2	0	0	0	2
Pre-requisite	NIL					Syllabus version
						v.1

Course Objectives:

The course gives students the necessary background to:

1. enable students to read and communicate in German in their day to day life
2. become industry-ready
3. make them understand the usage of grammar in the German Language.

Expected Course Outcome:

The students will be able to

1.create the basics of German language in their day to day life.
2.understand the conjugation of different forms of regular/irregular verbs.
3.understand the rule to identify the gender of the Nouns and apply articles appropriately.
4.apply the German language skill in writing corresponding letters, E-Mails etc.
5.create the talent of translating passages from English-German and vice versa and To frame simple dialogues based on given situations.

Module:1	**3 hours**

Einleitung, Begrüssungsformen, Landeskunde, Alphabet, Personalpronomen, Verb Konjugation, Zahlen (1-100), W-fragen, Aussagesätze, Nomen – Singular und Plural

Lernziel:

Elementares Verständnis von Deutsch, Genus- Artikelwörter

Module:2	**3 hours**

Konjugation der Verben (regelmässig /unregelmässig) die Monate, die Wochentage, Hobbys, Berufe, Jahreszeiten, Artikel, Zahlen (Hundert bis eine Million), Ja-/Nein- Frage, Imperativ mit Sie

Lernziel :

Sätze schreiben, über Hobbys erzählen, über Berufe sprechen usw.

Module:3	**4 hours**

Possessivpronomen, Negation, Kasus- AkkusatitvundDativ (bestimmter, unbestimmterArtikel), trennnbare verben, Modalverben, Adjektive, Uhrzeit, Präpositionen, Mahlzeiten, Lebensmittel, Getränke

Lernziel :

Sätze mit Modalverben, Verwendung von Artikel, über Länder und Sprachen sprechen, über eine Wohnung beschreiben.

Module:4	**6 hours**

Übersetzungen : (Deutsch – Englisch / Englisch – Deutsch)

Lernziel :

Grammatik – Wortschatz – Übung

Module:5	**5 hours**

Leseverständnis,Mindmap machen,Korrespondenz- Briefe, Postkarten, E-Mail

Lernziel : Wortschatzbildung und aktiver Sprach gebrauch		
Module:6	.	**3 hours**
Aufsätze : Meine Universität, Das Essen, mein Freund oder meine Freundin, meine Familie, ein Fest in Deutschland usw		
Module:7		**4 hours**
Dialoge: a) Gespräche mit Familienmitgliedern, Am Bahnhof, b) Gespräche beim Einkaufen ; in einem Supermarkt ; in einer Buchhandlung ; c) in einem Hotel - an der Rezeption ;ein Termin beim Arzt. Treffen im Cafe		
Module:8		**2 hours**
Guest Lectures/Native Speakers / Feinheiten der deutschen Sprache, Basisinformation über die deutschsprachigen Länder		
	Total Lecture hours:	**30 hours**

Text Book(s)	
1.	**Studio d A1 Deutsch als Fremdsprache, Hermann Funk, Christina Kuhn, Silke Demme : 2012**
Reference Books	
1	Netzwerk Deutsch als Fremdsprache A1, Stefanie Dengler, Paul Rusch, Helen Schmtiz, Tanja Sieber, 2013
2	Lagune ,Hartmut Aufderstrasse, Jutta Müller, Thomas Storz, 2012.
3	Deutsche SprachlehrefürAUsländer, Heinz Griesbach, Dora Schulz, 2011
4	ThemenAktuell 1, HartmurtAufderstrasse, Heiko Bock, MechthildGerdes, Jutta Müller und Helmut Müller, 2010
	www.goethe.de wirtschaftsdeutsch.de hueber.de klett-sprachen.de www.deutschtraning.org

Mode of Evaluation: CAT / Assignment / Quiz / Seminar / FAT			
Recommended by Board of Studies	04-03-2016		
Approved by Academic Council	41	Date	17-06-2016

Course code	Course Title	L	T	P	J	C
FRE5001	FRANCAIS FONCTIONNEL	2	0	0	0	2
Pre-requisite	Nil					Syllabus version
						1.0

Course Objectives:

The course gives students the necessary background to:

1. demonstrate competence in reading, writing, and speaking basic French, including knowledge of vocabulary (related to profession, emotions, food, workplace, sports/hobbies, classroom and family).
2. achieve proficiency in French culture oriented view point.

Expected Course Outcome:

The students will be able to

1. remember the daily life communicative situations via personal pronouns, emphatic pronouns, salutations, negations, interrogations etc.
2. create communicative skill effectively in French language via regular / irregular verbs.
3. demonstrate comprehension of the spoken / written language in translating simple sentences.
4. understand and demonstrate the comprehension of some particular new range of unseen written materials.
5. demonstrate a clear understanding of the French culture through the language studied.

Module:1	Saluer, Se présenter, Etablir des contacts	**3 hours**

Les Salutations, Les nombres (1-100), Les jours de la semaine, Les mois de l'année, Les Pronoms Sujets, Les Pronoms Toniques, La conjugaison des verbes réguliers, La conjugaison des verbes irréguliers- avoir / être / aller / venir / faire etc.

Module:2	**Présenter quelqu'un, Chercher un(e) correspondant(e), Demander des nouvelles d'une personne.**	**3 hours**

La conjugaison des verbes Pronominaux, La Négation, L'interrogation avec 'Est-ce que ou sans Est-ce que'.

Module:3	**Situer un objet ou un lieu, Poser des questions**	**4 hours**

L'article (défini/ indéfini), Les prépositions (à/en/au/aux/sur/dans/avec etc.), L'article contracté, Les heures en français, La Nationalité du Pays, L'adjectif (La Couleur, l'adjectif possessif, l'adjectif démonstratif/ l'adjectif interrogatif (quel/quelles/quelle/quelles), L'accord des adjectifs avec le nom, L'interrogation avec Comment/ Combien / Où etc.,

Module:4	**Faire des achats, Comprendre un texte court, Demander et indiquer le chemin.**	**6 hours**

La traduction simple :(français-anglais / anglais –français)

Module:5	**Trouver les questions, Répondre aux questions générales en français.**	**5 hours**

L'article Partitif, Mettez les phrases aux pluriels, Faites une phrase avec les mots donnés, Exprimez les phrases données au Masculin ou Féminin, Associez les phrases.

Module:6	**Comment ecrire un passage**	**3 hours**
Décrivez : La Famille /La Maison, /L'université /Les Loisirs/ La Vie quotidienne etc.		
Module:7	**Comment ecrire un dialogue**	**4 hours**
Dialogue: d) Réserver un billet de train e) Entre deux amis qui se rencontrent au café f) Parmi les membres de la famille g) Entre le client et le médecin		
Module:8	**Invited Talk: Native speakers**	**2 hours**
	Total Lecture hours:	**30 hours**

Text Book(s)	
1.	Echo-1, Méthode de français, J. Girardet, J. Pécheur, Publisher CLE International, Paris 2010.
2	Echo-1, Cahier d'exercices, J. Girardet, J. Pécheur, Publisher CLE International, Paris 2010.
Reference Books	
1.	CONNEXIONS 1, Méthode de français, Régine Mérieux, Yves Loiseau,Les Éditions Didier, 2004.
2	CONNEXIONS 1, Le cahier d'exercices, Régine Mérieux, Yves Loiseau, Les Éditions Didier, 2004.
3	ALTER EGO 1, Méthode de français, Annie Berthet, Catherine Hugo, Véronique M. Kizirian, Béatrix Sampsonis, Monique Waendendries , Hachette livre 2006.

Mode of Evaluation: CAT / Assignment / Quiz / Seminar / FAT			
Recommended by Board of Studies	26.02.2016		
Approved by Academic Council	No.41	Date	17-06-2016

Course code	Course Title	L	T	P	J	C
SET 5001	SCIENCE, ENGINEERING AND TECHNOLOGY PROJECT– I	0	0	0		2

Pre-requisite		**Syllabus Version**
Anti-requisite		1.10

Course Objectives:

- To provide opportunity to involve in research related to science / engineering
- To inculcate research culture
- To enhance the rational and innovative thinking capabilities

Expected Course Outcome:

On completion of this course, the student should be able to:

1. Identify problems that have relevance to societal / industrial needs
2. Exhibit independent thinking and analysis skills
3. Demonstrate the application of relevant science / engineering principles

Modalities / Requirements

1. Individual or group projects can be taken up
2. Involve in literature survey in the chosen field
3. Use Science/Engineering principles to solve identified issues
4. Adopt relevant and well-defined / innovative methodologies to fulfill the specified objective
5. Submission of scientific report in a specified format (after plagiarism check)

Student Assessment : Periodical reviews, oral/poster presentation

Recommended by Board of Studies	17-08-2017		
Approved by Academic Council	No. 47	Date	05-10-2017

Course code	Course Title	L	T	P	J	C
SET 5002	SCIENCE, ENGINEERING AND TECHNOLOGY PROJECT– II	0	0	0	0	2
Pre-requisite		Syllabus Version				
Anti-requisite		1.10				

Course Objectives:

1. To provide opportunity to involve in research related to science / engineering
2. To inculcate research culture
3. To enhance the rational and innovative thinking capabilities

Expected Course Outcome:

On completion of this course, the student should be able to:

1. Identify problems that have relevance to societal / industrial needs
2. Exhibit independent thinking and analysis skills
3. Demonstrate the application of relevant science / engineering principles

Modalities / Requirements

1. Individual or group projects can be taken up
2. Involve in literature survey in the chosen field
3. Use Science/Engineering principles to solve identified issues
4. Adopt relevant and well-defined / innovative methodologies to fulfill the specified objective
5. Submission of scientific report in a specified format (after plagiarism check)

Student Assessment : Periodical reviews, oral/poster presentation

Recommended by Board of Studies	17-08-2017		
Approved by Academic Council	No. 47	Date	05-10-2017

Course code	Course title	L	T	P	J	C
STS 5001	Essentials of Business Etiquette and problem solving	3	0	0	0	1
Pre-requisite	None					Syllabus version

Course Objectives:

1. To develop the students' logical thinking skills
2. To learn the strategies of solving quantitative ability problems
3. To enrich the verbal ability of the students
4. To enhance critical thinking and innovative skills

Expected Course Outcome:

1. Enabling students to use relevant aptitude and appropriate language to express themselves
2. To communicate the message to the target audience clearly
3. The students will be able to be proficient in solving quantitative aptitude and verbal ability questions of various examinations effortlessly

Module:1	Business Etiquette: Social and Cultural Etiquette and Writing Company Blogs and Internal Communications and Planning and Writing press release and meeting notes	9 hours

Value, Manners, Customs, Language, Tradition, Building a blog, Developing brand message, FAQs', Assessing Competition, Open and objective Communication, Two way dialogue, Understanding the audience, Identifying, Gathering Information, Analysis, Determining, selecting plan, Progress check, Types of planning, Write a short, catchy headline, Get to the Point – summarize your subject in the first paragraph., Body – Make it relevant to your audience,

Module:2	Study skills – Time management skills	3 hours

Prioritization, Procrastination, Scheduling, Multitasking, Monitoring, working under pressure and adhering to deadlines

Module:3	Presentation skills – Preparing presentation and Organizing materials and Maintaining and preparing visual aids and Dealing with questions	7 hours

10 Tips to prepare PowerPoint presentation, Outlining the content, Passing the Elevator Test, Blue sky thinking, Introduction , body and conclusion, Use of Font, Use of Color, Strategic presentation, Importance and types of visual aids, Animation to captivate your audience, Design of posters, Setting out the ground rules, Dealing with interruptions, Staying in control of the questions, Handling difficult questions

Module:4	Quantitative Ability -L1 – Number properties and Averages and Progressions and Percentages and Ratios	11 hours

Number of factors, Factorials, Remainder Theorem, Unit digit position, Tens digit position, Averages, Weighted Average, Arithmetic Progression, Geometric Progression, Harmonic Progression, Increase & Decrease or successive increase, Types of ratios and proportions

Module:5	**Reasoning Ability-L1 – Analytical Reasoning**	**8 hours**
Data Arrangement (Linear and circular & Cross Variable Relationship), Blood Relations, Ordering/ranking/grouping, Puzzle test, Selection Decision table		
Module:6	**Verbal Ability-L1 – Vocabulary Building**	**7 hours**
Synonyms & Antonyms, One-word substitutes, Word Pairs, Spellings, Idioms, Sentence completion, Analogies		
	Total Lecture hours:	**45 hours**

Reference Books	
1.	Kerry Patterson, Joseph Grenny, Ron McMillan, Al Switzler (2001) Crucial Conversations: Tools for Talking When Stakes are High. Bangalore. McGraw-Hill Contemporary
2.	Dale Carnegie, (1936) How to Win Friends and Influence People. New York. Gallery Books
3.	Scott Peck. M (1978) Road Less Travelled. New York City. M. Scott Peck.
4.	FACE (2016) Aptipedia Aptitude Encyclopedia. Delhi. Wiley publications
5.	ETHNUS (2013) Aptimithra. Bangalore. McGraw-Hill Education Pvt. Ltd.
Websites:	
1.	www.chalkstreet.com
2.	www.skillsyouneed.com
3.	www.mindtools.com
4.	www.thebalance.com
5.	**www.eguru.ooo**

Mode of Evaluation: FAT, Assignments, Projects, Case studies, Role plays,
3 Assessments with Term End FAT (Computer Based Test)

Course code	Course title	L	T	P	J	C
STS 5002	Preparing for Industry	3	0	0	0	1
Pre-requisite	None					Syllabus version
						1
Course Objectives:	1. To challenge students to explore their problem-solving skills 2. To develop essential skills to tackle advance quantitative and verbal ability questions 3. To have working knowledge of communicating in English					
Expected Course Outcome:	1. Enabling students to simplify, evaluate, analyze and use functions and expressions to simulate real situations to be industry ready. 2. The students will be able to interact confidently and use decision making models effectively 3. The students will be able to be proficient in solving quantitative aptitude and verbal ability questions of various examinations effortlessly					
Module:1	**Interview skills – Types of interview and Techniques to face remote interviews and Mock Interview**					**3 hours**
Structured and unstructured interview orientation, Closed questions and hypothetical questions, Interviewers' perspective, Questions to ask/not ask during an interview, Video interview¸ Recorded feedback, Phone interview preparation, Tips to customize preparation for personal interview, Practice rounds						
Module:2	**Resume skills – Resume Template and Use of power verbs and Types of resume and Customizing resume**					**2 hours**
Structure of a standard resume, Content, color, font, Introduction to Power verbs and Write up, Quiz on types of resume, Frequent mistakes in customizing resume, Layout - Understanding different company's requirement, Digitizing career portfolio						
Module:3	**Emotional Intelligence - L1 – Transactional Analysis and Brain storming and Psychometric Analysis and Rebus Puzzles/Problem Solving**					**12 hours**
Introduction, Contracting, ego states, Life positions, Individual Brainstorming, Group Brainstorming, Stepladder Technique, Brain writing, Crawford's Slip writing approach, Reverse brainstorming, Star bursting, Charlette procedure, Round robin brainstorming, Skill Test, Personality Test, More than one answer, Unique ways						
Module:4	**Quantitative Ability-L3 – Permutation-Combinations and Probability and Geometry and mensuration and Trigonometry and Logarithms and Functions and Quadratic Equations and Set Theory**					**14 hours**
Counting, Grouping, Linear Arrangement, Circular Arrangements, Conditional Probability, Independent and Dependent Events, Properties of Polygon, 2D & 3D Figures, Area & Volumes,						

Heights and distances, Simple trigonometric functions, Introduction to logarithms, Basic rules of logarithms, Introduction to functions, Basic rules of functions, Understanding Quadratic Equations, Rules & probabilities of Quadratic Equations, Basic concepts of Venn Diagram		
Module:5	**Reasoning ability-L3 – Logical reasoning and Data Analysis and Interpretation**	**7 hours**
Syllogisms, Binary logic, Sequential output tracing, Crypto arithmetic, Data Sufficiency, Data interpretation-Advanced, Interpretation tables, pie charts & bar chats		
Module:6	**Verbal Ability-L3 – Comprehension and Logic**	**7 hours**
Reading comprehension, Para Jumbles, Critical Reasoning (a) Premise and Conclusion, (b) Assumption & Inference, (c) Strengthening & Weakening an Argument		
	Total Lecture hours:	**45 hours**
References	• Michael Farra and JIST Editors(2011) Quick Resume & Cover Letter Book: Write and Use an Effective Resume in Just One Day. Saint Paul, Minnesota. Jist Works • Daniel Flage Ph.D(2003) The Art of Questioning: An Introduction to Critical Thinking. London. Pearson • FACE(2016) Aptipedia Aptitude Encyclopedia.Delhi. Wiley publications	
Mode of Evaluation: FAT, Assignments, Projects, Case studies, Role plays, 3 Assessments with Term End FAT (Computer Based Test)		

Course Code	Course Title	L	T	P	J	C
ECE6099	Masters Thesis	0	0	0	0	16
Pre-requisite	As per the academic regulations	Syllabus version				
		1.0				

Course Objectives:

To provide sufficient hands-on learning experience related to the design, development and analysis of suitable product / process so as to enhance the technical skill sets in the chosen field.

Expected Course Outcome:

At the end of the course the student will be able to

1. Formulate specific problem statements for ill-defined real life problems with reasonable assumptions and constraints.
2. Perform literature search and / or patent search in the area of interest.
3. Conduct experiments / Design and Analysis / solution iterations and document the results.
4. Perform error analysis / benchmarking / costing
5. Synthesise the results and arrive at scientific conclusions / products / solution
6. Document the results in the form of technical report / presentation

Contents

Capstone Project may be a theoretical analysis, modeling & simulation, experimentation & analysis, prototype design, fabrication of new equipment, correlation and analysis of data, software development, applied research and any other related activities.
Project should be for two semesters based on the completion of required number of credits as per the academic regulations.

Should be individual project.

In case of group projects, the individual project report of each student should specify the individual's contribution to the group project.

Carried out inside or outside the university, in any relevant industry or research institution.

Publications in the peer reviewed journals / International Conferences will be an added advantage

Mode of Evaluation: Periodic reviews, Presentation, Final oral viva, Poster submission

Recommended by Board of Studies	10-06-2015		
Approved by Academic Council	No. 37	Date	16-06-2015

Course Code	Course Title	L	T	P	J	C
ECE5014	ASIC DESIGN	3	0	2	0	4
Pre-requisite	Nil					

Course Objective :

The course is aimed to

1. explain the types of ASIC and typical ASIC design Flow.
2. give the students an understanding of HDL coding guidelines and synthesizable HDL constructs.
3. explain the RTL synthesis Flow with respect to different cost function.
4. teach the various timing parameter and how to perform Static Timing Analysis for ASIC chips.
5. discuss the various abstraction levels in physical design and guidelines at each abstraction level.
6. provide detailed insight on importance of physical design verification

Expected Course Outcome :

At the end of the course the student will be able to

1. Understand different types of ASICs and design flows.
2. Design digital systems by adhering to synthesizable HDL constructs.
3. Synthesize the given design by considering various constraints and to optimize the same.
4. Understand various timing parameters and compute computation time for a given design using static timing analysis.
5. Perform physical design by adhering to guidelines.
6. Apprehend the importance of physical design verification.
7. Design ASIC based systems using industry standard tools.

Module:1	ASIC Design Methodology & Design Flow	4 hours

Implementation Strategies for Digital ICs: Custom IC Design- Cell-based Design Methodology - Array based implementation approaches - Traditional and Physical Compiler based ASIC Flow.

Module:2	Verilog HDL Coding Style for Synthesis	6 hours

HDL Coding style – Guidelines and Recommendation - FSM Coding Guideline and Coding Style for Synthesis.

Module:3	RTL Synthesis	8 hours

RTL synthesis Flow – Synthesis Design Environment & Constraints – Architecture of Logic Synthesizer - Technology Library Basics– Components of Technology Library –Synthesis Optimization- Technology independent and Technology dependent synthesis- Data path Synthesis – Low Power Synthesis – Timing driven synthesis- Formal Verification.

Module:4	Timing Parameters	5 hours

Timing Parameter Definition – Setup Timing Check- Hold Timing Check- Multicycle Paths- False Paths - Clocking of Synchronous Circuits.

Module:5	Static Timing Analysis	7 hours

Timing Analysis - Clock skew optimization – Clock Tree Synthesis.

Module:6	Physical Design	8 hours

Detailed step in Physical Design Flow- Guidelines for Floor plan, Placement and routing. Conducting layers and their characteristics - Cell-based back-end design –ECO – Packaging- Layout Issues-Preventing electrical overstress.

Module:7	**Physical Design Verification**	**5 hours**
Static verification techniques-Post-layout design verification.		
Module:8	**Contemporary issues:**	**2 hours**
	Total Lecture hours:	**45 hours**

Text Book(s)	
1.	HimanshuBhatnagar, Advanced ASIC Chip Synthesis, Kluwer Academic Publisher, Second Edition, 2012.
Reference Books	
1.	Erik Brunvand, Digital VLSI Chip Design with Cadence and Synopsys CAD Tools, Addison Wesley, First Edition, 2010.
2.	J. Bhasker and RakeshChadha, Static Timing Analysis for Nanometer Designs, Springer US, First Edition, 2010.

Mode of Evaluation:Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).

List of Challenging Experiments (Indicative)		
1.	**Phase- I Design of digital architecture** Design Specification: Starting with the soda machine dispenser design described in lecture, create a block diagram and high-level state machine for a soda machine dispenser that has a choice of two soda types, and that also provides change to the consumer. A coin detector provides the circuit with a 1-bit input c that becomes 1 for one clock cycle when a coin is detected, and an 8-bit input a indicating the coin's value in cents. Two 8-bit input s1 and s2 indicate the cost of the two soda choices. The user's soda selection is controlled by two buttons b1 and b2 that when pushed will output 1 for one clock cycle. If the user has inserted enough change for their selection, the circuit should set either output bit d1 or d2 to 1 for one clock cycle, causing the selected soda to be dispensed. The soda dispenser circuit should also set an output bit cr to 1for one clock cycle if change is required, and should output the amount of change required using on an 8-bit output ca. Use the RTL design method to convert the high-level state machine to a controller and a data path. Design the data path to structure, but design the controller to the point of an FSM only.	12 hours
2.	**Phase-II Logical Synthesis of digital architecture** Apply design and timing constraints : Timing constraints: set_clock ,set_clock_uncertainty, set_clock_latency, set_clock_transition, set_input_delay, set_output_delay, set_false_path and set_multicycle_path. DRC constraints are: set_max_fanout, set_max_transition and set_max_capacitance. Optimization constraints :set_max_area, set_min_area, set_max_leakegeandset_max_dynamic.	6 hours
3.	**Phase-III Netlist Optimization and Formal Verification** Apply power optimization constraints, Gate Level Simulation and Formal verification of digital architecture.	4 hours
4.	**Phase-IV Physical Synthesis of digital architecture** create_floorplan, set_propgated_clock,preroute_standard_cells, set_route_zrt.	4 hours

5.	**Phase - VPhysical Verification of digital architecture** set_fix_multiple_port_nets, write_physical_constraints and write_parasitics	4 hours
	Total Laboratory hours:	30 hours
Mode of Evaluation: Continuous assessment of challenging experiments /Final Assessment Test (FAT).		
Recommended by Board of Studies	13-12-2015	
Approved by Academic Council	No. 40	18-03-2016

Course Code	Course Title	L	T	P	J	C
ECE5015	DIGITAL IC DESIGN	3	0	0	4	4
Pre-requisite	Nil					

Course Objective :

The course is aimed to

1. apply the models for state-of-the-art VLSI components, fabrication steps, hierarchical design flow and semiconductor business economics to judge the manufacturability of a design and assess its manufacturing costs.
2. focus on the systematic analysis and design of basic digital integrated circuits in CMOS technology.
3. enhance problem solving and creative circuit design techniques.
4. emphasize on the layout design of various digital integrated circuits.
5. focus on the methodologies and design techniques related to digital integrated circuits.

Expected Course Outcome :

At the end of the course the student will be able to

1. Understand design metric and MOS physics
2. Design layout for various digital integrated circuits.
3. Design the CMOS inverter with optimized power, area and timing.
4. Design static and dynamic digital CMOS circuits.
5. Understand the timing concepts in latch and flip-flops.
6. Design CMOS memory arrays.
7. Understand interconnect and clocking issues.

Module:1	Introduction:	3 hours

Issues in Digital IC Design- Quality Metrics of a Digital Design - MOS Transistor Theory.

Module:2	Fabrication Technologies:	7 hours

VLSI Manufacturing Process Steps - Crystal Growth - Wafer cleaning – Oxidation - Thermal Diffusion - Ion Implantation – Lithography –Epitaxy – Metallization -Dry and Wet etching and Packaging.

Fabrication of MOSFET with Metal Gate and Self-aligned Poly-Gate Processes with details on CMOS Design Rules and Layouts, Fabrication of CMOS inverter with details on Design Rules and Layouts.

Module:3	The CMOS Inverter:	5 hours

Static CMOS Inverter- Static and Dynamic Behavioural Practices of CMOS Inverter – Noise Margin.

Components of Energy and Power – Switching -Short-Circuit and Leakage Components.

Technology scaling and its impact on the inverter metrics - Passive and Active Devices.

Module:4	Static & Dynamic CMOS Design:	8 hours

Complementary CMOS -Ratioed Logic (Pseudo NMOS, DCVSL) - Pass Transistor Logic - Transmission gate logic - Dynamic Logic Design Considerations - Speed and Power Dissipation of Dynamic logic -Signal integrity issues -Domino Logic.

Module:5	CMOS Sequential Logic Circuit Design:	5 hours

Introduction - Static Latches and Registers - Dynamic Latches and Registers - Pulse Based

Registers - Sense Amplifier based registers -Latch vs. Register based pipeline structures.		
Module:6	**Designing Memory & Array structures:**	**7 hours**
SRAM and DRAM Memory Core - memory peripheral circuitry - Memory reliability and yield - Power dissipation in memories.		
Module:7	**Interconnects and Timing Issues:**	**8 hours**
Resistive, Capacitive and Inductive Parasitics - Computation of R, L and C for given inter-connects - Buffer Chains - Timing classification of digital systems - Synchronous Design - Origins of Clock Skew/Jitter and impact on Performance - Clock Distribution Techniques - Latch based clocking - Synchronizers and Arbiters -Clock Synthesis and Synchronization using a Phase-Locked Loop.		
Module:8	**Contemporary issues:**	**2 hours**
	Total Lecture hours:	**45 hours**

Text Book(s)	
1.	Jan M. Rabaey, AnanthaChadrakasan, BorivojeNikolic, Digital Integrated Circuits: A Design Perspective, PHI, Second Edition, 2016.
2.	Neil.H, E.Weste, David Harris, Ayan Banerjee, CMOS VLSI Design: A Circuit and Systems Perspective, Pearson Education, Fourth Edition, 2011.
Reference Books	
1.	Sung-Mo Kang, Yusuf Leblebici, CMOS Digital Integrated Circuits - Analysis and Design, McGraw-Hill, Fourth Edition, 2014.
2.	Sorab K Gandhi, VLSI Fabrication Principles: Si and GaAs, John Wiley and Sons, Second Edition, 2010.

Mode of Evaluation:Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).

List of Projects (Indicative)

1. Design and simulate a 16-bit comparator by using 8T full adders
2. Pass transistor logic based ALU design using low power full adder design
3. Design of high performance power efficient flip-flop using transmission gates
4. Design of high performance 5:32 decoder using 2:4,3:8 mixed logic line decoders.
5. Design of current comparator using FINFET
6. Analysis of leakage current and leakage power reduction during reduction in CMOS SRAM cell
7. Design of encoder for a 5GS/S 5 bit flash ADC
8. Design a 65 nm reliable 6T CMOS SRAM cell with minimum size transistors

Mode of Evaluation:Review I, II and III

Recommended by Board of Studies	13-12-2015	
Approved by Academic Council	No. 40	18-03-2016

Course Code	Course Title	L	T	P	J	C
ECE5016	ANALOG IC DESIGN	3	0	2	0	4
Pre-requisite	Nil					

Course Objectives :

The course is aimed to

1. analyze and design single-ended and differential IC amplifiers.
2. understand the relationships between devices, circuits and systems.
3. emphasize the design of practical amplifiers, small systems and their design parameter trade-offs.

Expected Course Outcome :

At the end of the course the student will be able to

1. Analyse low-frequency characteristics of single-stage amplifiers and differential amplifiers.
2. Analyse high-frequency response and noise of amplifiers.
3. Understand the feedback concepts.
4. Analyse and Design of High Gain Amplifiers.
5. Understand stability analysis and frequency compensation techniques of amplifiers.
6. Understand the basic concepts, non-idealities and applications of PLLs.
7. Design and characterize amplifiers according to design specifications in Cadence CAD software.

Module:1	Current source and Amplifier design:	8 hours

MOS Device models, MOS Current Sources and Sinks, Current Mirror: Basic Current Mirrors, Cascode current Mirrors. Bandgap references. Single stage Amplifies: Basic concepts, Common Source stage, Common Gate stage, Cascode stage. Differential stage: Single ended and Differential operation. Basic Differential Pair.

Module:2	Frequency response and Noise analysis of Amplifiers:	8 hours

Miller effect, Frequency response of Common Source stage, Common Gate stage, Cascode stage and Differential pair. Noise in Amplifiers: Common Source stage, Common Gate stage, Cascode stage, Differential pair. Noise Bandwidth.

Module:3	Feedback Amplifiers:	7 hours

Ideal feedback equation, Gain sensitivity, Effect of Negative Feedback on Distortion, Types of Feedback Amplifiers. Feedback configurations: voltage-voltage, current-voltage, current-current, voltage-current feedback. Practical configurations and Effect of loading.

Module:4	Operational Amplifier	8 hours

Common mode Feedback circuits, Op Amp CMRR requirements, Need for Single and Multistage amplifiers, Effect of loading in Differential stage. Performance Analysis: DC gain, Frequency response, Noise, Mismatch, Slew rate of cascode and two stage Op Amps, Fully Differential Op Amps, Common-Mode feedback loop stability.

Module:5	Stability analysis	4 hours

Basic Concepts, Instability and the Nyquist Criterion, Stability Study for a Frequency-Selective Feedback Network, Effect of Pole Locations on Stability

Module:6	**Frequency compensation**	**4 hours**
Frequency Compensation: Concepts and Techniques for Frequency Compensation – Dominant pole, Miller Compensation, Compensation of Miller RHP Zero, Nested Miller, Compensation of two stage OP Amps.		
Module:7	**Phase Locked Loops**	**4 hours**
Problem of Lock acquisition, Phase Detector, Basic PLL and its dynamics, Charge-pump PLL, Non-ideal effects in PLL: PFD/CL non idealities, Jitter, Delay Locked Loop, Applications.		
Module:8	**Contemporary issues:**	**2 hours**
	Total Lecture hours:	**45 hours**

Text Book(s)	
1.	BehzadRazavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill, Second Edition, 2017.
2.	David Johns and Ken Martin, Analog Integrated Circuit Design, John Wiley & Sons, Inc., Second Edition, 2012.
Reference Books	
1.	Phillip E. Allen and Douglas R. Holberg, CMOS Analog Circuit Design, Oxford University Press, UK, Second Edition, 2010.
2.	R. Jacob Baker, CMOS Circuit Design, Layout and Simulation, IEEE Press Series on Microelectronic Systems, Wiley Publications, Third Edition, 2010.

Mode of Evaluation:Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).

List of Challenging Experiments (Indicative)		
1	Analysis and Design of Common Source Amplifier with Diode Connected Load and Suggest a Circuit to achieve higher gain.	4 hours
2	Analysis and Design of Common Gate Amplifier with Resistive load and Current Source load. Justify the results in terms of input impedance of the circuit.	4 hours
3	Analysis and Design of Simple Current Mirror and Suggest a circuit to minimize the error in the output current.	4 hours
4	Analysis and Design of Differential Amplifier with Active load and Current Source Load.	6 hours
5	Analysis and Design of Cascode Amplifier and Suggest a Circuit to overcome Voltage Headroom Limitation.	4 hours
6	Analysis and Design of Two-Stage Opamp with Frequency Compensation.	8 hours
	Total Laboratory hours:	30 hours

Mode of Evaluation:Continuous assessment of challenging experiments /Final Assessment Test (FAT).

Recommended by Board of Studies	13-12-2015	
Approved by Academic Council	No. 40	18-03-2016

Course Code	Course Title	L	T	P	J	C
ECE5017	DIGITAL DESIGN WITH FPGA	2	0	2	4	4
Pre-requisite	Nil					

Course Objectives :

The course is aimed to

1. understand the various abstraction levels in Verilog HDL and thus model tasks & functions at behavioral level.
2. model the state machines using D and JK Flip Flops and design the complex combinational and sequential logic circuits using various constructs in Verilog.
3. understand the types programmable logic devices and building blocks of FPGA and thus implement the design using Xilinx and ALTERA FPGAs.

Expected Course Outcome :

At the end of the course the student will be able to

1. Understand various abstraction levels in Verilog HDL.
2. design finite state machine using D and JK Flip Flop.
3. model sequential circuit using behavioural modelling.
4. Design the complex combinational and sequential logic circuits using various constructs in Verilog.
5. Understand programmable logic devices and various blocks exist in FPGA.
6. distinguish the architectural and resource difference between ALTERA and Xilinx.
7. use EDA tool to design complex combinational and sequential circuits.
8. develop and prototype digital systems design using FPGA.

Module:1	Verilog HDL – Data Flow & Structural Modeling	6 hours

Lexical Conventions - Ports and Modules – Operators - Gate Level Modeling - Data Flow Modeling - System Tasks & Compiler Directives - Test Bench.

Module:2	State Machine Design	4 hours

Definition of state machines -State machine as a sequential controller- Analysis of state machines using D and JK flip-flops - Design of state machines- State table and State assignment - Transition/excitation table - excitation maps and equations - logic realization- Design examples: Sequence detector, Serial adder, Vending machine.

Module:3	Verilog HDL – Behavioral Modeling	5 hours

Behavioral level Modeling- Procedural Assignment Statements- Blocking and Non-Blocking Assignments -Tasks & Functions - Useful Modeling Techniques.

Module:4	Verilog Modeling of Combinational Circuits	4 hours

Behavioral, Data Flow and Structural Realization of Adders and Multipliers

Module:5	Verilog Modeling of Sequential Circuits	4 hours

Synchronous and Asynchronous FIFO – Single port and Dual port ROM and RAM - FSM Verilog modeling of Sequence detector - Serial adder - Vending machine.

Module:6	FPGA Architecture	3 hours

Types of Programmable Logic Devices: PLA, PAL, CPLD - FPGA Architecture - Programming Technologies-Chip I/O- Programmable Logic Blocks- Fabric and Architecture of FPGA.

Module:7	**Xilinx and ALTERA FPGAs**	**2 hours**
Xilinx Virtex 5.0 Architecture - Xilinx Virtex VI Architecture – ALTERA Cyclone II Architecture - ALTERA Stratix IV Architecture.		
Module:8	**Contemporary issues:**	**2 hours**
	Total Lecture hours:	**30 hours**

Text Book(s)

1.	Ming-Bo Lin, Digital Systems Design and Practice: Using Verilog HDL and FPGAs, Create Space Independent Publishing Platform, Second Edition, 2015.
2.	Michael D Ciletti, Advanced Digital Design with the Verilog HDL, Prentice Hall, Second Edition, 2011.

Reference Books

1.	Wayne Wolf, FPGA Based System Design, Prentices Hall Modern Semiconductor Design Series, 2011.
2.	Charles H Roth Jr, Lizy Kurian John and Byeong Kil Lee Digital Systems Design using Verilog, Cengage Learning, First Edition, 2016.

Mode of Evaluation: Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).

List of Challenging Experiments (Indicative)

1.	Many ink-jet printers have six cartridges for different colored ink: black, cyan, magenta, yellow, light cyan and light magenta. A multibit signal in such a printer indicates selection of one of the colors. Write a data flow Verilog model for a decoder for use in the inkjet printer described above. The decoder has three input bits representing the choice of color cartridge and six output bits, one to select each cartridge. Verify the output of the design using test bench by simulating in Modelsim Simulator. Implement the design in ALTERA DE2-115 Board and verify it's functionality.	**4 hours**
2.	Write a behavioral Verilog code to divide the ALTERA DE2-115 Board clock frequency 50MHz by 40MHZ, 30MHz, 20 MHz, 10MHz. Display each of the output using LEDs available in the board.	**4 hours**
3.	Design and implement a circuit on the DE2-115 board that acts as a time-of-day clock. It should display the hour (from 0 to 23) on the 7-segment displays HEX7−6, the minute (from 0 to 60) on HEX5−4 and the second (from 0 to 60) on HEX3−2. Use the switches SW15−0 to preset the hour and minute parts of the time displayed by the clock.	**4 hours**
4.	We wish to implement a finite state machine (FSM) that recognizes two specific sequences of applied input symbols, namely four consecutive 1s or four consecutive 0s. There is an input w and an output z. Whenever w = 1 or w = 0 for four consecutive clock pulses the value of z has to be 1; otherwise, z = 0. Overlapping sequences are allowed, so that if w = 1 for five consecutive clock pulses the output z will be equal to 1 after the fourth and fifth pulses. Design and Implement the design using DE2-115 Board.	**8 hours**
5.	Write a behavioral Verilog code to design FIFO with the following specification	**10 hours**

	d_in: input data; 8 bit width is considered d_out: output data; 8 bit width is considered · w_en: write enable signal r_en: read enable signal r_next_en: read next enable w_next_en: write next enable w_clk: write clock; 10 MHz for this design r_clk: read clock; 50 MHz for this design w_ptr: write address pointer; 4 bit to address depth of 16 · r_ptr: read address pointer; 4 bit to address depth of 16 · ptr_diff: address pointer difference; 4 bit width f_full_flag: FIFO full flag; asserted when FIFO is full · f_empty_flag: FIFO empty flag; asserted when FIFO is empty Use Dual Port RAM available in ALTERA IP library to realize the FIFO. Implement the design using ALTERA DE2-115 board.	
		Total Laboratory hours: 30 hours

Mode of Evaluation: Continuous assessment of challenging experiments / Final Assessment Test (FAT).

List of Projects (Indicative)

1. Design MIPS 32-Bit RISC Processor and implement it using ALTERA Cyclone IV FPGA and study about it's performance.
2. Design a Reconfigurable FIR Filter and verify it's functionality through test bench. Implement the design using ALTERA Cyclone IV FPGA.
3. Design and Implementation of Smart Traffic Light System for congested four way road using ALTERA Cyclone IV FPGA.
4. Design and Implementation of CORDIC Algorithm using ALTERA Cyclone IV FPGA.

Mode of Evaluation: Review I , II & III

Recommended by Board of Studies	13-12-2015	
Approved by Academic Council	No. 40	18-03-2016

Course code	Course Title	L	T	P	J	C
ECE 5018	Physics of VLSI Devices	3	0	0	0	3
Pre-requisite	None	Syllabus version				
		v.1.1				

Course Objectives :

The course is aimed to

1. Expound the fundamentals of intrinsic, extrinsic semiconductors with carrier concentration, modeling and physics of various carrier current transport mechanisms
2. Introduce detailed physics and modeling of PN Junction, MOS capacitors, and MOSFETs
3. Review and discuss in detail the short channel effects and the issues of UDSM transistors

Expected Course Outcome :

At the end of the course the student will be able to

1. Design extrinsic semiconductors with specific carrier concentrations and, understand the band structure and diagrams of semiconductors.
2. Calculate and model the carrier transport mechanism in semiconductors.
3. Model PN- junctions of given specifications
4. Model MOS capacitors
5. Model MOSFETs and model the MOSFETs
6. Mitigate the short channel effects and design UDSM transistors

Module:1	Semiconductor Physics	5 hours

Energy bands in solids - Intrinsic and Extrinsic semiconductors - Direct and Indirect bandgap - Density of states - Fermi distribution -Free carrier densities - Boltzmann statistics - Thermal equilibrium.

Module:2	Carrier Transport in Semiconductors	4 hours

Current flow mechanisms: Drift current, Diffusion current - Mobility of carriers - Current density equations - Continuity equation.

Module:3	P-N Junctions	5 hours

Thermal equilibrium physics - Energy band diagrams - Space charge layers - Poisson equation - Electric fields and Potentials - p-n junction under applied bias - Static current-voltage characteristics of p-n junctions - Breakdown mechanisms.

Module:4	MOS Capacitor	8 hours

Accumulation - Depletion - Strong inversion - Threshold voltage - Contact potential - Gate work function - Oxide and Interface charges - Body effect - C-V characteristics of MOS

Module:5	MOSFETs and Compact Models	8 hours

Drain current - Saturation voltage - Sub-threshold conduction - Effect of gate and drain voltage on carrier mobility - Compact models for MOSFET and their implementation in SPICE: Level 1, 2 and 3 - MOS model parameters in SPICE.

Module:6	Scaling and Short Channel Effects	6 hours

Effect of scaling - Channel length modulation - Punch-through - Hot carrier degradation - MOSFET breakdown - Drain-induced barrier lowering.

Module:7	**UDSM Transistor Design Issues**	**7 hours**
Effect of tox - Effect of high-k and low-k dielectrics on the gate leakage and Source and drain leakage - tunneling effects - Different gate structures in UDSM - Impact and reliability challenges in UDSM.		
Module:8	**Contemporary issues:**	**2 hours**
Total Lecture hours:		**45 hours**

Text Book(s)	
1.	Ben G. Streetman and S. Banerjee, Solid State Electronic Devices, Pearson Education, U.S, Seventh Edition, 2014.
2.	J.P. Colinge and C. A. Colinge, Physics of Semiconductor Devices, Kluwer Academic Publishers, US, 2017.
Reference Books	
1.	Y.P. Tsividis and Colin McAndrew, Operation and Modelling of the MOS Transistor, Oxford University Press, US, Third Edition, 2011.
2.	M K Achutan and K N Bhatt, Fundamental of Semiconductor Devices, McGraw Hill Education, US, 2017.
Mode of Evaluation: CAT / Assignment / Quiz / FAT	

Recommended by Board of Studies	05-10-2017		
Approved by Academic Council	No. 47		05-10-2017

Course Code	Course Title	L	T	P	J	C
ECE5019	COMPUTER AIDED DESIGN FOR VLSI	3	0	0	0	3
Pre-requisite	Nil					

Course Objective :

The course is aimed to

1. imbibe the students with the fundamentals of graphs, the relevance and, their applications to VLSI design automation.
2. introduce the students with relevant examples the estimation of computational complexity and the general classes of computational problems.
3. explain With relevant examples and algorithms demonstrate partitioning, floor planning, area routing, clock routing and pin assignment of physical design flow

Expected Course Outcome :

At the end of the course students will be able to

1. Formulate the graphs for the given problems;
2. Calculate and analyse the computational complexity of physical design algorithms;
3. Partition a given design.
4. Express and change the floorplans in an abstract manner and use computer algorithms to make large and optimized floorplans
5. Make optimized placements on the silicon chip and perform complex routing using algorithms and computer codes.
6. Design clock trees to distribute the clock signals on the chip while satisfying various constraints like clock skew and wire length.

Module:1	Introduction to course	5 hours

Y Chart- Physical design top down flow- Review of graph theory: complete graph, connected graph, sub graph, isomorphism, bi partite graph tree.

Module:2	Computational complexity of algorithms	4 hours

Big-O notation- Class P- class NP -NP-hard- NP-complete.

Module:3	Partitioning	6 hours

Problem formulation- Group Migration Algorithm: Kernighan-Lin Simulated annealing based Partitioning.

Module:4	Floor planning	6 hours

Stock Meyer algorithm- Wong-Liu algorithm (Normalized polish expression)- Integer Linear Programming (ILP) based floor planning.

Module:5	Pin Assignment and Placement	7 hours

Pin Assignment: Concentric circle mapping, Topological pin assignment- Power and ground routing.

Placement: Wire length estimation models for placement - Quadratic placement- Sequence pair technique.

Module:6	Routing	8hours

Routing: Grid routing- Maze routing- Line Probe algorithms, Weighted Steiner tree approach. Global routing: Rectilinear routing(spanning tree, steiner tree)-Dijkstra's algorithm-routing by ILP Detailed routing: Problem formulation- Two layer channel routing : Left Edge algorithm, Dogleg router- Net Merge channel router - Three-layer channel routing - HVH, VHV router- Introduction to switch box routing.		
Module:7	**Clocking Tree Topologies**	**7hours**
Clocking tree topologies: H-tree, Xtree- Method of Means and Medians (MMM)- recursive geometric matching- Elmore delay model to calculate skew- Buffer insertion in clock trees- Exact Zero skew clock routing algorithm. Clock mesh topologies: uniform and non-uniform mesh.		
Module:8	**Contemporary issues:**	**2hours**
	Total Lecture hours:	**45hours**
Text Book(s)		
1.	Andrew B. Kahng, Jens Lienig, Igor L. Markov, JinHu,VLSI Physical Design: From Graph Partitioning to Timing Closure, Springer, 2011.	
2	H. Yosuff and S.M. Sait, VLSI Physical Design Automation – Theory and Practice, Cambridge India, 2010.	
3.	Sung Kyu Lim, Practical Problems in VLSI Physical Design Automation, Springer India, 2011.	
Reference Books		
1.	S. Sridhar, Design and Analysis of Algorithms, Paperback – OUP, 2014.	
2.	John OkyereAttia, PSPICE and MATLAB for Electronics: An Integrated Approach,CRC Press, 2010.	
3.	Ganesh M.Magar, Swati R.Maurya Rajesh K.Maurya, Graph Theory & Applications, Technical Publications, 2016.	
4	Brian Christian and Tom Griffiths , Algorithms to Live By: The Computer Science of Human Decisions, William Collins, 2017.	
Mode of Evaluation:Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).		
Recommended by Board of Studies	13-12-2015	
Approved by Academic Council	No. 40	18-03-2016

Course Code	Course Title	L	T	P	J	C
ECE5020	DSP ARCHITECTURES	2	0	0	4	3
Pre-requisite	Nil					

Course Objective:

The course is aimed to

1. Explore different Digital Signal Processor (DSP) architectures and to design systems using programmable DSPs.
2. Improve system performance using different pipelining techniques, processor array and systolic array.
3. Interface of memory and peripherals to a DSP; and acquire knowledge on different codec implemented on DSP.

Expected Course Outcome:

The students will be able to

1. Identify and use specific Digital Signal Processor for various applications.
2. Design a system using programmable DSP.
3. Implement pipelining techniques to improve system performance.
4. Implement applications using processor array and systolic arrays to enhance the performance.
5. Design involving memory and other interfaces to DSP.
6. Design of various codecs on target DSPs.

Module:1	DSP Integrated Circuits and VLSI Technologies	2hours

Standard digital signal processors - Application specific IC's for DSP - DSP systems - DSP system design - Integrated circuit design.

Module:2	Architectures for programmable DSP	4 hours

Basic Architectural Features - DSP Computational Building Blocks - Bus Architecture and Memory - Data Addressing Capabilities - Address Generation Unit - Programmability and Program Execution - Features for External Interfacing.

Module:3	Execution Control and Pipelining	4 hours

Hardware looping – Interrupts – Stacks - Relative Branch support - Pipelining and Performance - Pipeline Depth – Interlocking - Branching effects - Interrupt effects - Pipeline Programming models.

Module:4	Synthesis of DSP Architectures	6 hours

Top Down approach to DSP LSI - Circuit Synthesis - High Performance Data conversion Techniques - LSI Algorithms and Architectures - Hierarchical Design of Processor Arrays - Systolic Arrays - Stack Filters - Wave-front Array Processors.

Module:5	Interfacing Memory and I/O to DSP Processors	5 hours

External bus interfacing signals - Memory interface - Parallel I/O interface - Programmed I/O - Interrupts and I/O -Direct memory access (DMA) A Multichannel buffered serial port (McBSP) - McBSP Programming.

Module:6	Interfacing CODEC	3 hours

CODEC interface circuit - CODEC programming - A CODEC-DSP interface example.

Module:7	**Multiprocessor Systems**	**4hours**
Architectures of Multiprocessors-Performance comparison of -Multiprocessor Structures.		
Module:8	**Contemporary issues:**	**2hours**
	Total Lecture hours:	**30hours**

Text Book(s)	
1.	Lars Wanhammer, DSP Integrated Circuits,Academic press, New York, 2011.
2.	Avtar Singh and S. Srinivasan, Digital Signal Processing, Thomson Publications, 2012.
Reference Books	
1.	Phil Lapsley, Jeff Bier, AmitShoham, Edward A. Lee, DSP Processor Fundamentals, Architectures & Features, Wiley-IEEE Press, First Edition,2011.
2.	Peter Pirsch, Architectures for Digital signal processing, Wiley India, 2010.

Mode of Evaluation: Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).

List of Projects (Indicative)

1. Image Compression algorithm implementation in Programmable DSP.
2. Image processing algorithm implementations on FPGA.
3. Turbo Decoder implementation.
4. CORDIC Algorithm implementation in PDSP/FPGA/ASIC flow.
5. Improved Adaptive filters.
6. Improved Median filters.

Mode of Evaluation: Review I, II and III

Recommended by Board of Studies	13-12-2015	
Approved by Academic Council	No. 40	18-03-2016

Course Code	Course Title	L	T	P	J	C
ECE5022	VLSI DIGITAL SIGNAL PROCESSING	3	0	0	0	3
Pre-requisite	Nil					

Course Objective :

The course aimed to:

1. Familiarise various representation methods of DSP algorithms, understand the significance of the iteration bound and to calculate the same for a given single-rate and/or multi-rate DFG.
2. Understand and apply the architectural transformation techniques such as retiming, unfolding and folding on a given DFG.
3. Introduce the algorithmic and numerical strength reduction methods for performance improvement.
4. Signify and calculate the effects of scaling and round-off noise for a given digital filter with limited word length.

Expected Course Outcome :

The students will be able to:

1. Compare various representation methods of DSP algorithms.
2. Find iteration bound of a given single and/or multi-rate DFG.
3. Understand and transform the given DFG using retiming with constraints.
4. Apply unfolding and folding transformations on the given DFG.
5. Understand and apply algorithmic and numerical strength reduction methods.
6. Understand and calculate scaling and round-off noise of the given digital filter with limited word length.

Module:1	Introduction to Digital Signal Processing	5 hours

Typical DSP Algorithms - DSP Application Demands and Scaled CMOS Technologies - Representations of DSP Algorithms - Data-Flow Graph Representations.

Module:2	Iteration Bound	5 hours

Introduction - Loop Bound and Iteration Bound - Algorithms for Computing Iteration Bound: Longest Path Matrix and Multiple Cycle Mean algorithms - Iteration Bound of Multi-rate Data Flow Graphs.

Module:3	Pipelining, Parallel processing and Retiming	8 hours

Pipelining and Parallel Processing - Introduction to Retiming - Definitions and Properties - Solving Systems of Inequalities - The Bellman-Ford Algorithm - The Floyd Warshall Algorithm- Retiming Techniques.

Module:4	Unfolding	6 hours

Introduction, An Algorithm for Unfolding, Properties of Unfolding, Critical Path, Unfolding, and Retiming, Applications of Unfolding.

Module:5	Folding	6 hours

Introduction, Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures.

Module:6	Algorithmic & Numerical Strength Reduction	7 hours

Introduction to Algorithmic Strength Reduction, Cook-Toom Algorithm, Iterated Convolution, Cyclic Convolution, Discrete Cosine Transform. Introduction to Numerical Strength

Reduction,Canonic Signed Digit Arithmetic, Sub-expression Elimination, Multiple Constant Multiplication, Sub-expression Sharing in Digital Filters.		
Module:7	**Scaling and Rounding Noise**	**6 hours**
Introduction, Scaling and Rounding Noise, State Variable Description of Digital Filters, Scaling and Rounding Noise Computation, Rounding Noise in Pipelined IIR Filters.		
Module:8	**Contemporary issues:**	**2 hours**
	Total Lecture:	**45 hours**
Text Book(s)		
1.	KeshabK.Parhi, VLSI Digital Signal Processing Systems: Design and Implementation,Reprint,Wiley, Inter Science, 2014.	
Reference Books		
1.	John G. Proakis, Dimitris K Manolakis, Digital Signal Processing: Principles, Algorithms and Applications, Prentice Hall, Fourth Edition, 2015.	
2.	Mohammed Ismail and Terri Fiez, Analog VLSI Signal and Information Processing,McGraw-Hill, 2014.	
3.	S.Y. Kung, H.J. White House, T. Kailath, VLSI and Modern Signal Processing, PHI, 2010.	
4.	S. K. Mitra, Digital Signal Processing – A Computer Based Approach, Fourth Edition, McGraw-Hill, 2010.	
Mode of Evaluation:Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).		
Recommended by Board of Studies	13-12-2015	
Approved by Academic Council	No. 40	18-03-2016

Course Code	Course Title	L	T	P	J	C
ECE5023	MEMORY DESIGN AND TESTING	3	0	0	0	3
Pre-requisite	Nil					

Course Objectives :

The course is aimed at

1. Expounding the basics and detailed architecture of SRAMs and DRAMs.
2. model the memory fault and introduce the basic and advanced memory testing patterns.
3. Elaborate the reliability and radiation effect issues of semiconductor memories and present methods for radiation hardening.
4. Review and discuss high performance memory subsystems, advanced memory technologies and contemporary issues

Expected Course Outcome :

At the end of the course the student should be able to

1. Design SRAMs and DRAMs.
2. Design NVRAMs and Flash Memories.
3. Model memory faults, select suitable testing patterns and develop testing patterns.
4. Incorporate DFT and BIST techniques for semiconductor memory testing.
5. Improve the reliability of semiconductor memories, simulate and model radiation effects and, perform radiation hardening.
6. Contribute to the development of high performance memory subsystems and use advanced memory technologies.

Module:1	Volatile memories	5 hours

SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, SOI technology, Advanced SRAM architectures and technologies, soft error failure in SRAM, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM.

Module:2	Non-volatile memories	5 hours

Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture.

Module:3	Memory Testing and Patterns	7 hours

General Fault Modeling – Read Disturb Fault Model – Precharge Faults – False Write Through Data Retention Faults – Decoder Faults. Megabit DRAM Testing Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing Application Specific Memory Testing – Zero/one Pattern – Exhaustive Test Patterns – Walking, Matching and Galloping – Pseudo Random Pattern – CAM pattern.

Module:4	Design For Test and BIST	4hours

RAM Built-In Self – Test (BIST)-Weak Write Test mode – Bit Line Contact Resistance – PFET Test – Shadow Write and Shadow Read.

Module:5	Reliability and Radiation Effects	7 hours

General Reliability Issues-RAM Failure Modes and Mechanism-Nonvolatile Memory Reliability-Design for Reliability Radiation Effects-Single Event Phenomenon (SEP)- Radiation Hardening Techniques Radiation Hardening Process and Design Issues-Radiation Hardened Memory Characteristics.		
Module:6	**High-Performance Subsystem Memories**	**7 hours**
Hierarchical Memory Systems, Memory-Subsystem Technologies, High-Performance Standard DRAMs, Embedded Memories.		
Module:7	**Advanced Memory Technologies**	**8 hours**
High-Density Memory Packaging Technologies, Ferroelectric Random Access Memories (FRAMs)- Analog Memories-Magneto-resistive Random Access Memories (MRAMs)-Experimental Memory Devices Memory Hybrids and MCMs (2D)- Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability.		
Module:8	**Contemporary issues:**	**2 hours**
	Total Lecture hours:	**45 hours**

Text Book(s)

1.	A. K.Sharma, Advanced Semiconductor Memories: Architecture, Design and Applications, John Wiley, 2014.
2.	Roberto Gastaldi and Giovanni Campardo In Search of the Next Memory: Inside the Circuitry from the Oldest to the Emerging Non-Volatile Memories, Springer, 2017.

Reference Books

1.	Alberto Bosio, Luigi Dilillo, Patrick Girard, Serge Pravossoudovitch, Arnaud Virazel, Advanced Test Methods for SRAMs: Effective Solutions for Dynamic Fault Detection in Nanoscaled Technologies, Springer, 2010.
2.	Hao Yu and YuhaoWang,Design Exploration of Emerging Nano-scale Non-volatile Memory, Springer, 2014.
3.	Takayuki Kawahara (Editor), Hiroyuki Mizuno (Editor), Green Computing with Emerging Memory: Low-Power Computation for Social Innovation, Springer, 2012.

Mode of Evaluation:Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).

Recommended by Board of Studies	13-12-2015	
Approved by Academic Council	No. 40	18-03-2016

Course Code	Course Title	L	T	P	J	C
ECE5024	IC TECHNOLOGY	3	0	0	0	3
Pre-requisite	Nil					

Course Objective :

The course is aimed to

1. Introduce the process involved in semiconductor manufacturing and fabrication.
2. Model the oxidation growth rate & to understand oxidation process and the process of diffusion and to expound the Ion Implantation process.
3. Explain the thin film deposition process and review the difference between MOS and Bipolar Process Integration.

Expected Course Outcome :

At the end of the course the student will be able to

1. Understand the process involved in semiconductor manufacturing and fabrication.
2. Understand the various lithography techniques used for pattern transfer.
3. Model the oxidation growth.
4. Model the diffusion mechanism in semiconductors.
5. Understand the process involved in thin film deposition.
6. Analyse the difference between MOS and Biploar Process.

Module:1	Crystal Growth	5 hours

Introduction to Semiconductor Manufacturing and fabrication, Clean Room types and Standards, Physics of the Crystal growth, wafer fabrication and basic properties of silicon wafers.

Module:2	Lithography:	7 hours

The Photolithographic Process, Photomask Fabrication, Comparison between positive and negative photoresists, Exposure Systems, Characteristics of Exposure Systems, E-beam Lithography, X- ray lithography.

Module:3	Thermal Oxidation of Silicon:	6 hours

The Oxidation Process, Modeling Oxidation, Masking Properties of Silicon Dioxide, Technology of Oxidation, Si-SiO2 Interface.

Module:4	Diffusion and Ion Implantation:	7 hours

The Diffusion Process , Mathematical Model for Diffusion, Constant- ,The Diffusion Coefficient , Successive Diffusions, Diffusion Systems, Implantation Technology, Mathematical Model for Ion Implantation, Selective Implantation, Channeling, Lattice Damage and Annealing, Shallow Implantations.

Module:5	**Thin film deposition, contacts, packaging and yield:**	**7 hours**
Chemical Vapor Deposition, Physical Vapor Deposition, Epitaxy, Metal Interconnections and Contact Technology, Silicides and Multilayer-Contact Technology, Copper Interconnects and Damascene Processes, Wafer Thinning and Die Separation, Die Attachment, Wire Bonding, Packages, Yield.		
Module:6	**MOS Process Integration:**	**5 hours**
Basic MOS Device Considerations, MOS Transistor Layout and Design Rules, Complementary MOS (CMOS) Technology.		
Module:7	**Bipolar Process Integration:**	**6 hours**
Isolation Techniques in BJT fabrication, Advanced Bipolar Structures, Other Bipolar Isolation Techniques. Deep Submicron Processes, Low-Voltage/Low-Power CMOS/BiCMOS Processes. Future Trends and Directions of CMOS/BiCMOS Processes.		
Module:8	**Contemporary issues:**	**2 hours**
	Total Lecture hours:	**45 hours**

Text Book(s)	
1.	S.M. Sze, VLSI technology, Tata McGraw-Hill, Second Edition, 2017.
2.	R.C. Jaeger, Introduction to microelectronic fabrication, Prentice Hall, Second Edition, 2013.
Reference Books	
1.	S.A. Campbell, The science and engineering of microelectronics fabrication, Oxford University Press, UK, Second Edition, 2012.
2.	Simon M. Sze, Gary S. May Fundamentals of Semiconductor Fabrication, Wiley, 2011.

Mode of Evaluation: Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).

Recommended by Board of Studies	13-12-2015	
Approved by Academic Council	No. 40	18-03-2016

Course Code	Course Title	L	T	P	J	C
ECE5025	SYSTEM ON CHIP DESIGN	3	0	0	0	3
Pre-requisite	Nil					

Course Objective :

The course is aimed to

1. Introducing design, optimization, and programing a modern System-on-a-Chip.
2. Detailing SoC design with on-chip memories and communication networks, I/O interfacing.
3. Making them understand about signal integrity aware SoC design and Scheduling algorithms.

Expected Course Outcome :

At the end of the course the student will be able to

1. Demonstrate an ability to identify, formulate and treat complex issues in the field of system-on-chip from a holistic perspective.
2. Improve the performance of SoC based design by various advanced techniques.
3. Apply SystemC for system design.
4. Use interconnection structures in a SoC / NoC based system design.
5. Apply static timing analysis for a SoC based design.
6. Analyse the cause and eliminate the issues relevant to signal integrity and scheduling.

Module:1	Introduction	3 hours

Architecture of the present-day SoC - Design issues of SoC- Hardware-Software Co design – Core Libraries – EDA Tools.

Module:2	Design Methodology for Logic, Memory and Analog Cores	6 hours

SoC Design Flow – guidelines for design reuse – Introduction- Efficiency of application specific hardware- Target architectures for HW/SW partitioning -System Integration, Embedded memories – design methodology for embedded memories – Specification of analog cores.

Module:3	Introduction to System C for SoC Design	7 hours

Co-Specification- System Partitioning- Co-simulation, Co-synthesis & Co-verification –SystemC and Co-specification and Co-simulation.

Module:4	SoC and NoC Interconnection Structures	7 hours

SoC Interconnection Structures- Bus-based Structures- AMBA Bus.Network on Chip -NoC Interconnection Structures-Topologies- routing- flow control- network components(router/switch, network interface, Links).

Module:5	STA for SoC Design	7 hours

Timing paths and its Timing Optimization- Slow to High and High to low frequency timing path- Half cycle timing path- Latch time borrowing- Interface Logic Model design and analysis for SoC design.

Module:6	Signal Integrity Aware SoC design	7 hours

Signal Integrity overview- EMI (Electro Magnetic Interference) and its protection- ESD and its Protection- Delay- Noise- glitches and its protection- Transmission lines- ringing. Crosstalk and

Glitch analysis-Types of Glitches- Glitch Threshold and propagation- Noise Accumulation with Multiple aggressor- Aggressor timing correlation- Crosstalk Delay analysis -Timing Verification using crosstalk delay-Positive and Negative crosstalk- aggressor victim timing correlation- aggressor victim functional correlation.		
Module:7	**Scheduling**	**6 hours**
Introduction and need for HLS- Major steps-Scheduling and Allocation- Binding/Assignment- Concept of Scheduling, Heuristic Scheduling Algorithm.		
Module:8	**Contemporary issues:**	**2 hours**
	Total Lecture hours:	**45 hours**

Text Book(s)	
1.	Michael J. Flynn, Wayne Luk,Computer System Design: System on chip,Wiley-Blackwell, First Edition, 2011.
2.	J. Bhasker, RakeshChadha,STA for Nanometer design – A practical approach, Springer, First Edition, 2010.
Reference Books	
1.	Jose L. Ayala,Communication Architectures for Systems-on-Chip, CRC Press, First Edition, 2011.
2.	Laung-Terng Wang, Charles E. Stroud, Nur A. Touba, System-on-Chip Test Architectures: Nanometer Design for Testability, Morgan Kaufmann, First Edition, 2010.
3.	Ahmed Jerraya and Wayne Wolf, Multiprocessor Systems-on-Chips (Systems on Silicon Series), Morgan Kaufmann, First Edition, 2010.

Mode of Evaluation:Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).		
Recommended by Board of Studies	13-12-2015	
Approved by Academic Council	No. 40	18-03-2016

Course Code	Course Title	L	T	P	J	C
ECE5026	SYSTEM DESIGN WITH FPGA	2	0	0	4	3
Prerequisite	Nil					

Course Objective :

This course is aimed to

1. review the fundamental concepts of C language.
2. expound the architecture of NIOS II soft core processor and the various peripheral interfaces used for system design.
3. implement the interconnect fabrics for the system and to design the system using NIOS II Soft core Processor.

Expected Course Outcome :

After completion of the course the student will be able to:

1. Understand the concepts of C language.
2. Understand the NIOS II soft core processor architecture.
3. Interpret the usage of various peripheral interfaces for system design.
4. Develop system by choosing suitable interconnect fabrics.
5. Design the system using NIOS II soft core processor.
6. Model the system by using IP block.
7. Design and develop embedded synthesis using FPGA.

Module:1	**Basic C Concepts**	**5 hours**
Loops, Arrays, structures, pointers, functions, linked list		
Module:2	**Soft Core Processor**	**5 hours**
Nios II Processor – Configurability Features – Processor Architecture-Instruction set		
Module:3	**Peripheral Interfaces**	**5 hours**
LCD, PS2, RS232, SDRAM, SRAM Controller, VGA, Audio and Video,PIO, External Bus bridge and IrDA		
Module:4	**NIOS II programming for peripheral Interfaces**	**4 hours**
LCD, PS2, RS232, SDRAM, SRAM, VGA, Audio, IrDA.		
Module:5	**Interconnect Fabrics**	**3 hours**
Avalon Switch Fabric Interconnect - Implementation and Functions- Integrated Design Environment		
Module:6	**System Design**	**4 hours**
Traffic light Controller, Real Time Clock - Interfacing using FPGA: VGA, , LCD, Camera		
Module:7	**IP Block Implementation**	**2 hours**
Edge detection algorithm, Colour and Brightness Enhancement algorithm		
Module:8	**Contemporary issues:**	**2 hours**
	Total Lecture hours:	**30 hours**

Text Book(s)		
1.	ZainalabedinNavabi, “Embedded Core Design with FPGAs”, TATA McGraw Hill Ltd, 2011.	
2.	Paul J. Deitel, Harvey M. Deitel, “C: How to Program”, Pearson Education, 2012	
Reference Books		
1	NIOS II Handbook, 2014.	
2	T.N.Padmanabhan,ThirupuraSundari, “Design Through VerilogHDL”,Wiley Student Edition, 2010.	
Mode of Evaluation:Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).		
TypicalProjects		
1. Implementation of edge detection algorithm 2. Implementation of self-guided vehicle. 3. Implementation of smart home system 4. Implementation of Health Monitoring System 5. Implementation of Music Synthesizer.		
Mode of Evaluation:Review I, II and III		
Recommended by Board of Studies	13-12-2015	
Approved by Academic Council	No. 40	18-03-2016

Course Code	Course Title	L	T	P	J	C
ECE5027	ADVANCED COMPUTER ARCHITECTURE	3	0	0	0	3
Pre-requisite	Nil					

Course Objective :

The course is aimed to

1. Introduce advanced concepts of computer architecture.
2. Acquire knowledge on various interconnect topology for multiprocessor system and different pipelining techniques.
3. Understanding different memory hierarchy for multiprocessor and multicomputer systems.

Expected Course Outcomes:

At the end of the course the student will be able to:

1. Understand the architecture of the various multiprocessors and multicomputer.
2. Identify possible parallel execution at hardware and software level.
3. Design required static or dynamic interconnect network for a multiprocessor system.
4. Apply different pipelining techniques to reduce computation time.
5. Analyse the various memory design for multiprocessor and multicomputer.
6. Design scalable parallel architecture for multiprocessor system.

Module:1	Parallel computer models	3 hours

cThe state of computing - Classification of parallel computers - Multiprocessors and Multicomputer - Multivector and SIMD computers.

Module:2	Program and network properties	7 hours

Conditions of parallelism - Data and resource Dependences - Hardware and software parallelism - Program partitioning and scheduling - Grain Size and latency - Program flow mechanisms - Control flow vs data flow - Data flow Architectures.

Module:3	System Interconnect Architectures	7 hours

Network properties and routing - Static interconnection Networks - Dynamic interconnection Networks - Multiprocessor system Interconnects - Hierarchical bus systems - Crossbar switch and multiport memory - Multistage and combining network.

Module:4	Pipelining	7 hours

Linear pipeline processor - nonlinear pipeline processor - Instruction pipeline Design - Mechanisms for instruction pipelining - Dynamic instruction scheduling - Branch Handling techniques - branch prediction - Arithmetic Pipeline Design

Module:5	Memory Hierarchy Design	6 hours

Cache basics & cache performance - reducing miss rate and miss penalty - multilevel cache hierarchies - main memory organizations - design of memory hierarchies.

Module:6	Shared Memory Architectures	7 hours

Symmetric shared memory architectures - distributed shared memory architectures - cache coherence protocols - scalable cache coherence - directory protocols - memory based directory protocols - cache based directory protocols.

Module:7	Multiprocessor Architectures	6 hours

Computational models - An Argument for parallel Architectures - Scalability of Parallel Architectures - Benchmark Performances.		
Module:8	**Contemporary issues:**	**2 hours**
	Total Lecture hours:	**45 hours**

Text Book(s)	
1.	Kai Hwang, NareshJotwani, Advanced Computer Architecture: Parallelism, Scalability, Programmability,Tata McGraw Hill Education Pvt. Ltd., India, Second Edition, 2011.
Reference Books	
1.	John L. Hennessy, David A. Patterson, Computer Architecture: A Quantitative Approach, Morgan Kaufmann, Fifth Edition, 2011.
2.	DezsoSima, Terence Fountain, PeterrKarsuk Advanced computer Architectures – A Design Space Approach, Pearson, 2014.
Mode of Evaluation:Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).	

Recommended by Board of Studies	13-12-2015	
Approved by Academic Council	No. 40	18-03-2016

Course Code	Course Title	L	T	P	J	C
ECE5028	MICROSENSORS AND INTERFACE ELECTRONICS	2	0	0	4	3
Pre-requisite	Nil					

Course Objective :

The course is aimed to

1. Introduce various types of Microsensors & micro actuators corresponding materials to fabricate it.
2. Make them Understand the concepts of Microsystem technologies used for realizing Microsensors and actuators.
3. Explore the working principles of interface electronics circuits for resistive, capacitive and temperature sensors.

Expected Course Outcome :

After the completion of the course, students will be able to:

1. Understand the Micro and Smart Systems.
2. Identify MEMS materials and Properties.
3. Understand the fabrication process flow for Microsystems.
4. Classify and Comprehend different types of Sensors and Actuators.
5. Explain about the wide applications of Microsensors.
6. Understand the basic Interface Circuits.
7. Understand the approach in design of Sensor Interface circuits.

Module:1	Introduction to Micro and Smart Systems	3 hours

Microsystems and scaling law, MEMS &Micro machines, Evolution of Microsystems, Silicon and Non-silicon Micro and Smart Systems, Market for Microsystems.

Module:2	Microsystem Materials and Properties	3 hours

Materials - Silicon, Silicon oxide and nitride, Thin Metal films (Cr, Au, Ti, Pt), Polymers (SU8, PMMA, PDMS), Glass and Quartz.

Important material properties-Young modulus, Poisson's ratio, density, piezoresistive coefficients, TCR, Thermal Conductivity, Material Structure.

Module:3	Micro System Technology	5 hours

Single Crystal Silicon Growth, Wafer Cleaning, Oxidation, Diffusion, Ion implantation, PVD, CVD, Electroplating, Lithography, Bulk Micromachining, Surface Micromachining, LIGA, Bonding and Packaging.

Module:4	Introduction to Sensors and Actuators	4 hours

Electrostatic, Piezoelectric, Piezoresistive, Electromagnetic, Thermo pneumatic, Shape Memory Alloy, Thermoelectric, Optical and Resonant.

Module:5	Applications of Micro Devices	4 hours

Industrial and Automotive Applications: Pressure Sensors, Accelerometers, Gas Sensors, Flow sensors, Gyroscopes, Micro mixer, Micro Valve, Micro Pump, Micro heater.

Telecommunication Applications: Imaging and Displays, Fiber optic communication devices.

Micro and Smart Systems -2. Biomedical Applications: Micro & Nano Cantilevers, Glucose sensors, In Vitro and In Vivo Diagnostics.RF Applications – Switches, Phase Shifters, Resonators and Varactors.

Module:6	**Interface Circuits**	**5 hours**
Interface circuits for Resistive, Capacitive and Temperature Sensors		
Module:7	**Voltage and Current - Mode Approach in Sensor Interfaces Design**	**4 hours**
Voltage-Mode Approach in Sensor Interfaces Design, DC & AC excitation for resistive sensors, capacitive sensor interfacing,temperature sensor interfaces. Current-Mode Approach in Sensor Interfaces Design, AC-Excitation Voltage for Resistive/Capacitive Sensors, DC-Excited Resistive Sensor Interface.		
Module:8	**Contemporary issues:**	**2 hours**
	Total Lecture hours:	**30 hours**

Text Book(s)	
1.	M. Madou, Fundamentals of Microfabrication and Nanotechnology, CRC Press, Third Edition, 2011.
2.	Anderia De Marcellis, Giuseppe ferri, Analog circuits and systems for voltage-mode and current-mode sensor interfacing applications, Springer, 2011.

Reference Books	
1.	N. Maluf, K Williams, An Introduction to Microelectromechanical Systems Engineering,Artech House Inc,Second Edition, 2004
2.	S. Senturia, Microsystem Design, Springer Publisher, 2007.
3.	MinhangBao, Analysis and Design Principles of MEMS Devices, Elsevier Science, 2005.
4.	G. Kovacs, Micromachined Transducers Sourcebook, McGraw-Hill, 1998

Mode of Evaluation: Continuous Assessment Test –I (CAT-I) ,Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).

List of Projects (Indicative)

1. Design of Piezoelectric cantilever for energy harvesting applications.
2. Fault detection using accelerometer and gyroscope.
3. Design of Silicon pressure sensors for car tire pressure monitoring.
4. PDMS pressure sensor for disposable blood pressure sensors.
5. PDMS grippers for the micromanipulation of biological cells.
6. Thermoactuator switches for optical signal control.
7. Design of Gas sensors for automobiles.

Mode of Evaluation:Review I , II & III

Recommended by Board of Studies	13-12-2015	
Approved by Academic Council	No. 40	18-03-2016

Course Code	Course Title	L	T	P	J	C
ECE5029	VLSI TESTING AND TESTABILITY	3	0	0	0	3
Pre-requisite	Nil					

Course Objective :

The course is aimed to

1. Model and simulate different types of faults in digital circuits at the gate level.
2. Establish equivalence and dominance relationships of faults in a circuit.
3. compare automatic test pattern generation algorithms with respect to search space, speed, fault coverage and other criteria.
4. Handle design complexity, ensure reliable operation, and achieve short time-to-market using various testing methodologies.

Expected Course Outcome :

After completion of the course students will be able to:

1. Model different fault models.
2. Simulate faults and generate test patterns for combinational circuits.
3. Apply scan based testing.
4. Recognize the BIST techniques for improving testability.
5. Understand boundary scan based test architectures.
6. Analyse and apply the test vector compression techniques for memory reduction and fault diagnosis.

Module:1	Fault Modelling	6hours

Importance of Testing - Testing during the VLSI Lifecycle - Challenges in the VLSI Testing: Test Generation - Fault Models - Levels of Abstraction in VLSI Testing - Historical Review of VLSI Test Technology - Functional Versus Structural Testing - Levels of Fault Models - Fault Equivalence - Fault Dominance - Fault Collapsing - Check point Theorem - Delay Fault.

Module:2	Fault Simulation and Test Generation	7hours

Fault Simulation: Serial, Parallel, Deductive, Concurrent - Combinational Test Generations - ATPG for Combinational Circuits - D-Algorithm - Testability Analysis - SCOAP measures for Combinational Circuits

Module:3	Scan based Testing	7hours

Design for Testability Basics - Ad Hoc Approach - Structured Approach - Scan Cell Designs - Scan Architectures - Scan Design Rules - Scan Design Flow – Special Purpose Scan Designs - RTL Design for Testability.

Module:4	Built-in Self-Test	7hours

BIST Design Rules - Test Pattern Generation - Exhaustive Testing - Pseudo-Random Testing - Pseudo-Exhaustive Testing - Delay Fault Testing - Output Response Analysis - Logic BIST Architectures - BIST Architectures for Circuits with and without Scan Chains

Module:5	Boundary scan and Core based Testing	5hours

Digital Boundary Scan (IEEE Std. 1149.1): Test Architecture and Operations - On-Chip Test Support with Boundary Scan - Board and System-Level Boundary-Scan Control Architectures.

Module:6	**Test Compression and Compaction**	**6hours**
Test Stimulus Compression: Code-Based Schemes, Linear-Decompression-Based Schemes - Test Response Compaction.		
Module:7	**Fault Diagnosis**	**5hours**
Dictionary Based and Adaptive fault diagnosis.		
Module:8	**Contemporary issues:**	**2hours**
	Total Lecture hours:	**45hours**
Text Book(s)		
1.	Z.Navabi, Digital System Test and Testable Design, Springer, 2011.	
1.	Laung-Terng Wang, Cheng-Wen Wu, and Xiaoqing Wen, VLSI Test Principles and Architectures, The Morgan Kaufmann, 2013.	
Mode of Evaluation:Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).		
Recommended by Board of Studies	13-12-2015	
Approved by Academic Council	No. 40	18-03-2016

Course code	Course Title	L	T	P	J	C
ECE 5030	Scripting languages for VLSI design automation	2	0	2	0	3
Pre-requisite	None	Syllabus version				
		v. 1.0				

Course Objectives :

The course is aimed to

1. To write scripts in the LINUX environment.
2. To study the principles of Scripting Languages like Perl, TCL and Python.
3. To write the scripts for automation using the languages like Perl, TCL and Python.

Expected Course Outcome :

At the end of the course the students will be able to

1. Work in LINUX environment.
2. Develop the PERL scriptts
3. Develop the TCL & TK scripts for automation
4. Develop the python scripts for automation
5. Write scripts for a given EDA design automation

Module:1	**LINUX Basics**	**3 hours**

Introduction to Linux, File System of Linux, General usage of Linux Kernel and Basic Commands, Linux users and group, Permissions for file, directory and users, Searching a file and directory, zipping and unzipping concepts.

Module:2	**PERL Basics**	**5 hours**

History and Concepts of PERL - Scalar Data - Arrays and List Data - Control structures – Hashes - Basics I/O - Regular Expressions – Functions - Miscellaneous control structures - Formats.

Module:3	**Advanced Topics in PERL**	**4 hours**

Directory access - File and Directory manipulation - Process Management - Packages and Modules.

Module:4	**TCL Basics**	**4 hours**

An Overview of TCL and Tk -Tcl Language syntax – Variables – Expressions – Lists - Control flow – procedures - Errors and exceptions - String manipulations.

Module:5	**Advanced Topics in TCL**	**4 hours**

Accessing files- Processes. Applications - Controlling Tools - Basics of Tk.

Module:6	**Python Basics**	**4 hours**

Introduction to Python – Using Python interpreter – Control flow Tools – Data structures – Modules

Module:7	**Advanced Topics in Python**	**4 hours**

Input and Output – Errors and Exceptions – Classes – Brief tour on standard library

Module:8	**Contemporary issues:**	**2 hours**
Total Lecture hours:		**30 hours**

Reference Books

1.	Guido van Rossum Fred L. Drake, Jr., editor, “Python Tutorial Release 3.2.3”, 2012.	
2.	Larry Wall, Tom Christiansen, John Orwant, “Programming PERL”, Oreilly Publications, Fourth Edition, 2012.	
3.	John K. Ousterhout, Ken Jones, “Tcl and the Tk Toolkit”, Pearson Education, Second Edition, 2010.	
Mode of Evaluation: CAT / Assignment / Quiz / FAT / Project / Seminar		
List of Challenging Experiments (Indicative)		
1.	Write a script to generate random test vectors for a given Verilog design.	3 hours
2.	Write a script which reads a verilog design module and identifies whether it is a sequential or combinational design. Accordingly, the perl script should generate the testbench file in verilog. Also, the input vectors from the testbench should be in a randomized fashion.	3 hours
3.	Write a script that reads a set of log files from different simulation directories and generates a consolidated report in .xls format which should contain the information of the test name, status and error messages. If the test is indicated as successful in the log file, the status in the report should be as “TEST PASSED” and if the test is unsuccessful, then the report should display the status as “TEST FAILED”.	2 hours
4.	Write a TCL Script which when executed should automatically compile your design modules and testbench modules and then perform the simulation. If the simulation is successful, then the script should synthesize the design module. The TCL script should also create a separate directory to dump the log files and a separate directory to write the netlist file.	3 hours
5.	Write a script to perform netlist patching.	2 hours
6.	Verification automation tool development using Perl/Python scripts	2 hours
Total Laboratory Hours		15 hours
Mode of evaluation: Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).		

Recommended by Board of Studies	05-03-2019		
Approved by Academic Council	No. 54	Date	14-03-2019

Course code	Course Title	L	T	P	J	C
ECE 6024	VLSI Verification Methodologies	2	0	0	4	3
Pre-requisite	ECE5017 Digital Design with FPGA	Syllabus version				
		v. 1.0				

Course Objective:

1. To introduce various verification techniques.
2. To write Testbench using System Verilog.
3. To develop UVM test bench environment

Expected Course Outcome :

The students will be able to :

1. Comprehend the VLSI verification techniques.
2. Define classes and create objects.
3. Develop design using system verilog.
4. Make Verification environment using System Verilog.
5. Cognize the UVM Verification environment.
6. Create reusable verification environment using UVM.

Module:1	Verification Techniques	4 hours

Introduction to Verification - Testing Vs Verification - Verification Technologies - Functional Verification- Code coverage – Functional coverage. Testbench – Linear Testbench - Linear Random Testbench - Self-checking Testbench – Regression - RTL Formal Verification.

Module:2	Basic OOP	3 hours

OOP Terminology, Creating Object, object deallocation, copying objects, static variables, Global variables, Inheritance, Polymorphism

Module:3	System Verilog – Data Types & Procedural statements	6 hours

Introduction to System Verilog – Literal values-data Types – Arrays – Array methods – Creating new types with typedef – user defined structures – Enumerated types – attributes - operators – expressions - Procedural statements and control flow - Processes in System Verilog – Task and functions – Routine arguments – Returning from a routine

Module:4	Connecting Testbench and Design	3 hours

Program, Interface, Stimulus timing, Module interactions, Connecting together, Development of self-checking test environment – Generator, Transactor, Driver, Monitor, Checker, Scoreboard

Module:5	Randomization, Assertion and Coverage	3 hours

Randomization in system Verilog, Constraints, Functional coverage, cross coverage, cover groups, Assertions

Module:6	Universal Verification Methodology	4 hours

Introduction to UVM - Verification components - Transaction level modeling

Module:7	UVM – Verification Environments	5 hours

Developing reusable verification components - Using Verification components – Developing reusable verification environment – Register classes.

Module:8	Contemporary issues:	2 hours

	Total Lecture hours:	**30 hours**

Reference Books:

1.	Vanessa R. Copper, “Getting started with UVM: A Beginner’s Guide”, Verilab Publishing, First Edition, 2013.
2.	Ray Salmei, “The UVM Primer: A Step-by-Step Introduction to the Universal Verification Methodology” Boston Light Press; First edition, 2013.
3.	Christian B Spear, “System Verilog for Verification: A guide to learning the Testbench language features”, Springer publications, Third Edition, 2012.
4.	Janick Bergeron, “Writing Testbenches using System Verilog” Synopsys Inc., Springer Publications, 2006.

Mode of Evaluation: CAT / Assignment / Quiz / FAT / Project / Seminar

List of Challenging Projects (Indicative)

1.	Develop a system Verilog testbench to verify your DUT by following the steps given below. i) Write the following blocks in system Verilog to verify your design a. Program Block b. Interface Block with clocking block and modport c. Top Level Harness file which has the instance of your DUT, test program and the interface. ii) Develop the Generator, Transactor and Driver components for your DUT iii) Develop the self-checking feature by writing the receiver, monitor and checker components for your DUT. iv) Simulate and verify the output.
2.	Define a packet class to encapsulate the packet information and create random packet objects in the generator then send, receive and check the correctness of the DUT using the packet objects for the given router IP. Follow the instructions given in the lab to complete the task. Simulate and verify the output for the good RTL code and the faulty code. Include covergroups and check the functional coverage is greater than 90%.

Mode of evaluation: Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).

Recommended by Board Of Studies	05-03-2019		
Approved by Academic Council	No. 54	Date	14-03-2019

Course Code	Course title	L	T	P	J	C
ECE6025	LOW POWER IC DESIGN	2	0	0	4	3
Pre-requisite	ECE5015 - Digital IC Design					

Course Objective :

The course is aimed to

1. Understand the concepts and techniques of Low power VLSI.
2. Develop a broad insight into the methods used to confront the low power issue from lower level (circuit level) to higher levels (system level) of abstraction.
3. develop a system with multiple supply and threshold voltages used for low power DSP applications.

Expected Course Outcome :

After completion of the course student will be able to:

1. Understand the factors affecting the power in VLSI circuits.
2. Apply algorithmic and architectural level power optimization methods.
3. Apply logic and circuit level power optimization techniques.
4. Apply register transfer level power optimization techniques.
5. Develop an optimum code to reduce the power in the software level.
6. Analyse and explore the usage of sleep transistors for low power.
7. Develop power efficient IPs.

Module:1	Introduction to Low Power Design Methods	3 hours

Motivation- Context and Objectives-Sources of Power dissipation in Ultra Deep Submicron CMOS Circuits – Static, Dynamic and Short circuit components Effects of scaling on power consumption- Low power design flow- Normalized Figure of Merit – PDP& EDP- Overview of power optimization at various levels.

Module:2	Algorithmic and Architecture Level Optimization	5hours

Pipelining and Parallel Processing approaches for low power in DSP filter structures- Multiple supply voltage and Multiple threshold voltage designs for low power- Computer arithmetic techniques for low power- Optimal drivers of high speed low power- software level power optimization.

Module:3	Logic Level and Circuit Level Optimization	5hours

Theoretical background – Calculation of Steady state probability- Transition probability - Conditional probability- Transition density- Estimation and optimization of Switching activity- Power cost computation model.

Transistor variable re-ordering for power reduction- Low power library cell design (GDI)- Estimation of glitching power- leakage power optimization-Subthreshold logic design.

Module:4	Register Transfer Level Optimization	4 hours

Low power clock-Interconnect and layout designs- Low power memory design and low power SRAM architectures- Clock gating- Bus Encoding techniques-Deglitching for low power.

Module:5	Low Power Design of Sub-Modules	5hours

Circuit techniques for reducing power consumption in Adders- Multipliers. Synthesis of FSM for

low power- Retiming sequential circuits for low power.		
Module:6	**Sleep Transistor Design**	**3hours**
Design metrics- switch efficiency- area efficiency- IR drop, normal Vs reverse body bias -Layout design of Area efficiency- Single row Vs double row- Inrush current and current latency.		
Module:7	**IP Design for Low Power**	**3hours**
Architecture and partitioning for power gating- power controller design for the USB OTG- Issues in designing portable power controllers- clocks and resets- Packaging IP for reuse with power intent.		
Module:8	**Contemporary issues:**	**2 hours**
	Total Lecture hours:	**30hours**

Text Book(s)

1.	Jan M.Rabaey, MassoudPedram, Low power Design methodologies,SpringerUS, First Edition, 2014.
2.	Kaushik Roy, Sharat Prasad, Low Power CMOS VLSI circuit design, John Wiley and Sons Inc, Second Edition,2010.

Reference Books

1.	Soudris, Dimitrios, ChristrianPignet, Goutis, Costas, Designing CMOS circuits for low power, Springer US, FirstEdition, 2011.
2.	Gary K.Yeap, Practical Low Power Digital VLSI Design, Springer US, First Edition 2010.
3.	AjitPal , Low Power VLSI circuits and Systems, Springer India, First Edition, 2014.

Mode of Evaluation:Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).

List of Projects (Indicative)

1. Design of Low Power, High Speed VLSI Adder and Multiplier Subsystems
2. Power Gating Design solutions for Low Power
3. Circuit level power reduction using multi-V_t
4. Non-conventional Low Power Circuits such as Energy Recovery Logic
5. Design of Low Power Clocking Solution for a Sequential System
6. Low power SRAM and CAM design
7. Low Power FFT Design for Wireless Communication Systems
8. Low Power Filter design for SDR systems.

Mode of Evaluation: Review I , II & III

Recommended by Board of Studies	13-12-2015	
Approved by Academic Council	No. 40	18-03-2016

Course Code	Course Title	L	T	P	J	C
ECE6026	MIXED SIGNAL IC DESIGN	2	0	0	4	3
Pre-requisite	ECE5016-Analog IC Design					

Course Objective:

The course is aimed to

1. introduce the design aspects of dynamic analog circuits and analog-digital interface electronics in CMOS technology.
2. Specify design implement ADC & DAC.

Expected Course Outcome :

At the end of the course the student will be able to

1. Understand the theory of discrete-time signal processing and its implementation using analog techniques.
2. Realizing Sample and Hold Circuits using MOS by considering the non-idealities.
3. Analyse CMOS based Switched Capacitor Circuits.
4. Understanding basics of Data Converters.
5. Analyse the architectures of ADCs and DAC.
6. Understand the oversampling converter architecture.
7. Gain mixed-signal design experience using Cadence EDA tools.

Module:1	Sampling	3hours

Introduction – sampling - Spectral properties of sampled signals - Oversampling – Anti-alias filter design. Time Interleaved Sampling - Ping-pong Sampling System - Analysis of offset and gain errors in Time Interleaved Sample and Hold.

Module:2	Sampling Circuits:	3 hours

Sampling circuits- Distortion due to switch - Charge injection - Thermal noise in sample and holds - Bottom plate sampling - Gate bootstrapped switch -Nakagome charge pump. Characterizing Sample and hold - Choice of input frequency.

Module:3	Switched Capacitor Circuits:	4hours

Switched Capacitor (SC) circuits– Parasitic Insensitive Switched Capacitor amplifiers - Non idealities in SC Amplifiers – Finite gain - DC offset - Gain Bandwidth Product. Fully differential SC circuits - DC negative feedback in SC circuits.

Module:4	A/D and D/A Converters Fundamentals:	2hours

Data converter fundamentals: Offset and gain Error - Linearity errors - Dynamic Characteristics – SQNR - Quantization noise spectrum.

Module:5	Analog to Digital Converter Architectures:	4 hours

Flash ADC - Regenerative latch - Preamp offset correction - Preamp Design - necessity of up-front sample and hold for good dynamic performance. Folding ADC - Multiple-Bit Pipeline ADCs and SAR ADC.

Module:6	Digital to Analog Converter Architectures:	5hours

DAC spectra and pulse shapes - NRZ vs RZ DACs. DAC Architectures: Binary weighted - Thermometer DAC - Current steering DAC - Current cell design in current steering DAC - ChargeScaling DAC - Pipeline DAC.

Module:7	**Oversampling Converter:**	**7hours**
Benefits of Oversampling -Oversampling with Noise Shaping - Signal and Noise Transfer Functions - First and Second Order Delta-Sigma Converters. Introduction to Continuous-time Delta Sigma Modulators - time-scaling - inherent antialiasing property - Excess Loop Delay - Influence of Op-amp nonidealities - Effect of Op-amp nonidealities - finite gain bandwidth - Effect of ADC and DAC nonidealities - Effect of Clock jitter.		
Module:8	**Contemporary issues:**	**2hours**
	Total Lecture hours:	**30hours**

Text Book(s)

1.	Frank Ohnhauser, Analog-Digital Converters for Industrial Applications Including an Introduction to Digital-Analog Converters Springer Publishers, First Edition, 2015.
2.	David Johns and Ken Martin, Analog Integrated Circuit Design, John Wiley & Sons Inc., 2012.

Reference Books

1.	Ahmed M.A.Ali, High Speed Data Converters IET Materials, Circuits & Devices, First Edition, 2016.
2.	S.Pavan,R. Schreier and Gabor.C.Temes, Understanding Delta – Sigma Data Converters, IEEE Press, First Edition, 2017.

Mode of Evaluation: Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).

Typical Projects

1. Design of Flash ADC
2. Design of High Speed Sample and Hold Amplifier.
3. Design of Charge Pump Circuit.
4. Design of Switched Capacitor Integrator
5. Design of Current – Steering DAC

Mode of Evaluation :Review I, II & III

Recommended by Board of Studies	13-12-2015	
Approved by Academic Council	No. 40	18-03-2016

Course Code	Course Title	L	T	P	J	C
ECE6027	RFIC DESIGN	2	0	0	4	3
Pre-requisite	ECE5016 - Analog IC Design					

Course Objectives:

The course is aimed at

1. To become familiarize with the design of integrated radio front-end circuits.

Expected Course Outcomes:

At the end of the course the student should be able to

1. Understand the concepts of RF IC Design.
2. Understand the High Frequency model of MOS and importance of Impedance Matching.
3. Analyse the various transceiver and radio architectures.
4. Design Low Noise amplifiers and Mixers with specifications.
5. Realize VCOs and Frequency synthesizers and their applications to transceiver design.
6. Classify and comprehend the design of Power Amplifiers.
7. Gain RFIC design experience in Cadence CAD tools.

Module:1	Introduction to RF & Wireless Technology:	5hours

Complexity design and applications - Choice of Technology - Basic concepts in RF Design: Nonlinearly - Time Variance - Intersymbol Interference - random processes - Noise. Definitions of sensitivity - dynamic range -conversion Gain and Distortion.

Module:2	High Frequency Model of RF Transistors and Matching Networks:	4hours

MOSFET behaviour at RF frequencies - Noise performance and limitation of devices - Impedance matching networks - transformers and baluns.

Module:3	Analog& Digital Modulation for RF Circuits:	4hours

Coherent and Non coherent detection - Mobile RF Communication systems and basics of Multiple Access techniques - Receiver and Transmitter Architectures and Testing: Heterodyne - Homodyne, Image-reject, Direct-IF and subsampled receivers - Direct Conversion and two steps transmitters.

Module:4	Low Noise Amplifiers and Mixers	4hours

Low Noise Amplifiers: Common Source LNA - Common Gate LNA -Cascode LNA. Mixers: Design of Active and Passive Mixers.

Module:5	Voltage Controlled Oscillators and Frequency Synthesizers:	3hours

Oscillators: Basic topologies VCO and definition of phase noise. Noise-Power trade-off. Resonatorless VCO design - Quadrature and single-sideband generators - Radio Frequency Synthesizers: PLLs.

Module:6	RF Power Amplifiers:	4hours

Class A, AB, B, C amplifiers - Class D, E, F amplifiers - RF Power amplifier design.

Module:7	Radio architectures:	4hours

GSM radio architectures, CDMA, UMTS radio architectures.

Module:8	**Contemporary issues:**	**2hours**
	Total Lecture hours:	**30hours**

Text Book(s)	
1.	B.Razavi, RF Microelectronics, Pearson Education Limited, Second Edition, 2013.
2.	HoomanDarabi, Radio-Frequency Integrated Circuits and Systems, Cambridge University Press, First Edition, 2015.
Reference Books	
1.	Gu, Qizheng, RF System Design of Transceivers for Wireless Communications, Springer, 2010
2.	Bosco Leung, VLSI for Wireless Communication, Springer, Second Edition, 2011

Mode of Evaluation:Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).

List of Projects(Indicative)

1. I-V Characterisation study of RF device/circuit
2. Design of Low Noise Amplifier
3. Design of Voltage Controlled Oscillators
4. Design of Power Amplifiers
5. Design and Implement- any one of the Receiver architecture

Mode of Evaluation: Review I, II & III

Recommended by Board of Studies	13-12-2015	
Approved by Academic Council	No. 40	18-03-2016

Course Code	Course Title	L	T	P	J	C
ECE6028	NANOSCALE DEVICES AND CIRCUIT DESIGN	2	0	0	4	3
Pre-requisite	ECE5018 - Physics of VLSI Devices					

Course Objective :

The course is aimed to

1. Make student to understand CMOS scaling
2. understand theory and operation of multigate MOSFET and analog design digital, circuits using multigate devicesaterials and their properties used for designing Microsensors.
3. understand the concepts of Microsystem technologies used for realizing Microsensors and actuators.
4. understand the working principles of Interface Electronic Circuits for resistive, capacitive and temperature sensors.

Expected Course Outcome :

At the end of the course the students will be able to

1. Understand the CMOS scaling
2. explain the need of novel MOSFET.
3. explain the physics of multigate MOS system
4. model nanowire FETs.
5. Design digital and analog circuit using multigate devices.
6. Understand the physics of CNTFET
7. Develop analytical model for novel FETs and validate them by numerical simulations..

Module:1	CMOS Scaling Issues and Solutions	2hours

MOSFET scaling, short channel effects, quantum effects, volume inversion, threshold voltage, channel engineering, source/drain engineering, high-k dielectric, strain engineering,multigate technology mobility, gate stack.

Module:2	Introduction to Novel MOSFETs	2hours

SOI MOSFET, multigate transistors, single gate, double gate, triple gate, surround gate, Silicon Nanowire transistors

Module:3	Physics of Multi-gate MOS System	5hours

MOS electrostatics, 1D, 2D MOS electrostatics, ultimate limits, double gate MOS system, gate voltage effect, semiconductor thickness effect, asymmetry effect, oxide thickness effect , electron tunnel current, two dimensional confinement, scattering

Module:4	Nanowire FETS	5hours

Silicon nanowire MOSFETs, evaluation of I-V characteristics, I-V characteristics for non-degenerate carrier statistics, I-V characteristics for degenerate carrier statistics, electronic conduction in molecules, general model for ballistic nano transistors, CNT-FETs

Module:5	Digital Circuit Design using Multi-gate Devices	5hours

Digital circuits design, impact of device performance on digital circuits, leakage performance trade off, multi VT devices and circuits, SRAM design

Module:6	Analog Circuit Design using Multi-gate Devices	5hours

Analog circuit design, trans-conductance, intrinsic gain, flicker noise, self-heating, band gap voltage reference, operational amplifier, comparator designs, mixed signal, successive approximation DAC, RF circuits		
Module:7	**Carbon Nanotube FET**	**4hours**
CNT-FET, CNT memories, CNT based switches, logic gates, CNT based RF devices, CNT based RTDs, CNTFET based applications		
Module:8	**Contemporary issues**	**2 hours**
	Total Lecture hours:	**30hours**

Text Book(s)	
1.	J P Colinge, FINFETs and other Multi-gate Transistors, Springer, Germany, 2010.
2.	B.G.Park, S.W. Hwang &Y.J.Park, Nanoelectronic Devices, Pan Stanford Publisher, Singapore, 2012.
Reference Books	
1.	N. Collaert, CMOS Nanoelectronics: Innovative Devices, Architectures and Applications, Reprint Pan Stanford publisher, Singapore, 2012.
2.	Niraj K. Jha, Deming Chen, Nanoelectronic Circuit Design, Springer London, First Edition, 2011.

Mode of Evaluation:Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / QUIZ, Final Assessment Test (FAT).

List of Projects

1. Design and Extraction of DC and AC parameters of MOSFET with Source/Drain Extension
2. Performance Analysis of Double/Triple/Surround gate devices
3. Analysis of Gate Work Function Engineering in Multi-gate Devices
4. Single Event Upset/Soft Error Analysis in Multi-gate FETs
5. Comparison of CMOS and Fin FET based SRAM
6. Design of OTA and Comparator in Multi-gate Devices

Mode of Evaluation:Review I, II & III

Recommended by Board of Studies	13-12-2015	
Approved by Academic Council	No. 40	18-03-2016