M.Tech – Embedded Systems

Curriculum and Syllabus

2020-21

VISION STATEMENT OF VELLORE INSTITUTE OF TECHNOLOGY

Transforming life through excellence in education and research.

MISSION STATEMENT OF VELLORE INSTITUTE OF TECHNOLOGY

World class Education: Excellence in education, grounded in ethics and critical thinking, for improvement of life.

Cutting edge Research: An innovation ecosystem to extend knowledge and solve critical problems.

Impactful People: Happy, accountable, caring and effective workforce and students.

Rewarding Co-creations: Active collaboration with national & internationalindustries & universities for productivity and economic development.

Service to Society: Service to the region and world through knowledge and compassion.

VISION STATEMENT OF THE SCHOOL OF ELECTRONICS ENGINEERING

To be a leader by imparting in-depth knowledge in Electronics Engineering, nurturing engineers, technologists and researchers of highest competence, who would engage in sustainable development to cater the global needs of industry and society.

MISSION STATEMENT OF THE SCHOOL OF ELECTRONICS ENGINEERING

- Create and maintain an environment to excel in teaching, learning and applied research in the fields of electronics, communication engineering and allied disciplines which pioneer for sustainable growth.
- Equip our students with necessary knowledge and skills which enable them to be lifelong learners to solve practical problems and to improve the quality of human life.

PROGRAMME EDUCATIONAL OBJECTIVES (PEOs)

The graduates of the programme will be able to

PEO 1 Excel in professional career and/or higher education by acquiring solid foundation in science, mathematics and advanced communication engineering and technologies.

PEO 2 Develop and apply engineering solutions for solving contemporary, social and human issues with realistic constraints suitable for the present need through the use of modern tools.

PEO 3 Exhibit professional and ethical standards, effective communication skills, teamwork spirit, multidisciplinary and transdisciplinary approach for successful careers and to be able to compete globally, function as leaders, as entrepreneurs, and manage information efficiently and to engage in lifelong learning.

PROGRAMME OUTCOMES (POs)

On completion of the Programme the students will have the

PO_01: Having an ability to apply mathematics and science in engineering applications.

PO_02: Having an ability to design a component or a product applying all the relevant standards and with realistic constraints, including public health, safety, culture, society and environment

PO_03: Having an ability to design and conduct experiments, as well as to analyse and interpret data, and synthesis of information

PO_04: Having an ability to use techniques, skills, resources and modern engineering and IT tools necessary for engineering practice

PO_05: Having problem solving ability- to assess social issues (societal, health, safety, legal and cultural) and engineering problems

PO_06: Having adaptive thinking and adaptability in relation to environmental context and sustainable development

PO_07: Having a clear understanding of professional and ethical responsibility

PO_08: Having a good cognitive load management skills related to project management and finance

Programme Specific Outcomes

On completion of M.Tech. Embedded Systems, graduates will be able to

PSO1. Apply the advanced concepts of Embedded System Design with real-time constraints using advanced Microcontrollers and FPGA based systems.

PSO2. Use the cutting-edge technologies in both hardware and software, to solve real-world multidisciplinary problems and arrive at a viable solution.

PSO3. Independently carry out research on diverse Embedded System strategies to address practical problems and present a substantial technical report.

School of Electronics Engineering (SENSE)

M.Tech - Embedded Systems

CURRICULUM

[Curriculum for Applied Learning (CAL)]

S. No.	Category	Total number of credits
1	University Core (UC)	27
2	University Elective (UE)	06
3	Programme Core (PC)	19
4	Programme Elective (PE)	18
	Total Credits	70

DETAILED CURRICULUM

University Core

S. No.	Course Code	Course Title	L	Т	Р	J	С
1.	MAT6001	Advanced statistical methods 2		0	2	0	3
	ENG5001 and	Fundamentals of communication Skills and Professional and communication Skills		0	2	0	
2.	ENG5002 or			0	2	0}	2
	FRE5001/ GER5001	(or) Foreign Languages	2	0	0	0	
3.	STS5001 & STS5002	Soft Skills	0	0	0	0	2
4.	SET 5001	SET Project – I	0	0	0	0	2
5.	SET 5002	SET Project – II	0	0	0	0	2
6.	ECE6099	Master's Thesis	0	0	0	0	16

University Elective

S. No.	Course Code	Course Title	L	Т	Р	J	С
1.		University Elective	0	0	0	0	6

Programme Core

S.No.	Course Code	Course Title	L	Т	P	J	С
1.	ECE5041	Embedded System Design	3	0	0	0	3
2.	ECE5042	Microcontroller Architecture and	2	0	2	4	4
		Organization					
3.	ECE5053	Electronic Hardware System Design	2	0	2	4	4
4.	ECE5043	Embedded Programming	3	0	2	0	4
5.	ECE5054	Real Time Operating System	3	0	2	0	4

Programme Elective

S.No.	Course Code	Course Code Course Title		Т	Р	J	С
1	ECE6036	In Vehicle Networking	3	0	0	0	3
2	ECE6042	Wireless and Mobile Communication	3	0	0	0	3
3	ECE6043	Advanced Processors and its applications	2	0	0	4	3
4	ECE6044	lectromagnetic Interference and Compatibility in SD 3			0	0	3
5	ECE5045	Advanced Digital Image Processing	3	0	0	0	3
6	ECE6037	Fault Tolerance and Dependable Systems	3	0	0	0	3
7	ECE6046	Advanced Embedded Programming		0	0	0	3
8	ECE6047	Design and Analysis of Algorithms	3	0	0	4	4
9	ECE6038	'irtual Instrumentation Systems		0	4	4	3
10	ECE6048	Embedded System design using FPGA	2	0	0	4	3
11	ECE5044	Hardware Software Co-design	3	0	0	0	3
12	ECE6049	Modern automotive electronics systems	2	0	0	4	3
13	ECE6073	6073 AUTOSAR and ISO Standards for Automotive Systems		0	0	0	2
14	ECE6092	Intelligent IoT System Design and Architecture		0	0	4	3
15	ECE6093	Advanced Machine Learning and Deep Learning	3	0	0	0	3
16	ECE6094	Scripting Languages for Design Automation	2	0	2	0	3
17	CSE6052	arallel Processing and Computing		0	0	0	3

University Core

	ADVANCED STATISTICAL N	AETHODS	L	Τ	P	J	С				
MAT6001											
Dave and and a to the	Nora		2	0	2	0	3				
Pre-requisite	None		2	syna	$\frac{\mathbf{ous}}{20}$	vers	sion				
Course Objective	s				2.0						
1. To provide	e students with a framework that wi	ll help them	choose	the	app	ropr	iate				
descriptive	descriptive statistics in various data analysis situations										
2. To analyse distributions and relationships of real-time data.											
3. To apply estimation and testing methods to make inference and modelling techniques for											
decision making using various techniques including multivariate analysis.											
At the end of the e	ourse the students, are expected to										
[1] understand	the concept of correlation and regre	ssion model a	nd ahle	e to i	nter	nret	the				
effect of variat	bles, regression coefficients, coefficient	of determination	na uono m.		mor	prot	the				
[2] make app	propriate decisions using inferential	statistical too	ls that	are	cer	ntral	to				
experimental r	esearch.										
[3] understan	d the statistical forecasting method	ls and model	fittin	g b	y gi	raph	ical				
interpretation of	of time series data.			1							
[4] construct	standard experimental designs and de	scribe what sta	atistica	l mo	dels	can	be				
[5] demonstrat	g the data.										
	e K programming for statistical data										
Module:1 Bas	sic Statistical Tools for Analysis:				4	4 ho	ours				
Summary Statistic	s, Correlation and Regression, Concept	of R ² and Adju	sted R	² and	Part	tial a	and				
Multiple Correlation	on, Fitting of simple and Multiple Linea	ır regression, E	xplana	tion a	ind						
Assumptions of Re	egression Diagnostics										
Modulov2 Sta	tistical information .					0 ho					
Basic Concepts	Normal distribution Area properties	Steps in tests	of sig	mific	ance						
sample tests-Z test	ts for Means and Proportions Small sa	mple tests –t-te	est for	Mear	ance is. F	test	for				
Equality of Varian	ces, Chi-square test for independence o	f Attributes.	50 101	liicui	10, 1	test	101				
Module:3 Mo	delling and Forecasting Methods:				(9 ho	urs				
Introduction: Con	cept of Linear and Non Liner For	ecasting mode	l ,Con	cepts	s of	Tre	end,				
Exponential Smoo	othing, Linear and Compound Growth	model, Fitting	g of Lo	ogisti	c cu	rve	and				
their Applications,	Moving Averages, Forecasting accurate	y tests.	[A maa	dala							
Probability mode	is for time series: Concepts of AR, AR		IA IIIO	uers.							
Module:4 Des	sign of Experiments:				(6 ho	ours				
Analysis of variar	nce – one and two way classifications	- Principle of	design	ofe	expei	rime	ents,				
CRD – RBD – LS	D, Concepts of 2^2 and 2^3 factorial exp	eriments.	-		-						
Module:5 Con	ntemporary Issues:				,	2 ho	ours				
Industry Expert Le	ecture	L									

		Total Lecture hours:	30 hours						
Tevt	Book(s)								
1. 1.	1. Applied Statistics and Probability for Engineers, Douglas C. Montgomery George C. Runger, 6 th edition, John Wiley & Sons (2016),								
2	Time S	eries Analysis and Its Applications With R Examples, Shum	way, Robert H.,						
	Stoffer,	David S., 4 th edition, Springer publications (2017)							
Refe	rence Bo	ooks							
1.	The Ele Hastie a	ements of Statistical Learning: Data Mining, Inference, and Pr and Robert Tibshirani, 2 nd Edition, Springer Series, (2017)	rediction, Trevor						
2	Introduce the Con (2017)	ction to Probability and Statistics: Principles and Applications for I nputing Sciences, J. Susan Milton and Jesse Arnold, McGraw Hill	Engineering and education						
Mod	e of Eva	luation							
1.100	Dig	ital Assignments, Quiz, Continuous Assessments, Final Assessme	ent Test						
List	of Chall	enging Experiments (Indicative)							
1.	Comput	ting Summary Statistics using real time data	3 hours						
2	Plotting Represe	g and visualizing data using Tabulation and Graphical entations.	3 hours						
3	Applyin dataset; scale da	ng simple linear and multiple linear regression models to real computing and interpreting the coefficient of determination for ta.	3 hours						
4.	Testing	of hypothesis for Large sample tests for real-time problems.	2 hours						
5.	Testing mean ar	of hypothesis for Small sample tests for One and Two Sample and paired comparison (Pre-test and Post-test)	2 hours						
6.	Testing	of hypothesis for Small Sample tests for F-test	2 hours						
7	Testing	of hypothesis for Small Sample tests for Chi-square test	2 hours						
8	Applyin models	ng Time series analysis-Trends. Growth ,Logistic, Exponential	2 hours						
9	Applyir Forecas	ng Time series model AR, ARMA and ARIMA and testing ting accuracy tests.	3 hours						
10	Perform real data	ing ANOVA (one-way and two-way), CRD, RBD and LSD for aset.	3 hours						
11	Perform	$\frac{1}{2^2}$ factorial experiments with real time Applications	2 hours						
12	Perform	$\frac{2^3}{1}$ factorial experiments with real time Applications	3 hours						
	1	Total Laboratory Hours	30 hours						

Mode of Evaluation									
Weekly Assessments, Final Assessment Test									
Recommended by Board of Studies	dies 25-02-2017								
Approved by Academic Council	No. 46	Date	24-08-2017						

ENG5001	Fundamentals of Communicat	ion Skills	L T P J C						
			0 0 2 0 1						
Pre-requisite	Not cleared EPT (English Proficiency Test)	Syllabus version						
			1.0						
Course Objective	Course Objectives:								
1. To enable learne	. To enable learners learn basic communication skills - Listening, Speaking, Reading and Writing								
2. To help learners	. To help learners apply effective communication in social and academic context								
3. To make studen	ts comprehend complex English language the	rough listening a	nd reading						
Expected Course	Expected Course Outcome:								
1. Enhance the list	ening and comprehension skills of the learne	rs							
2.Acquire speaking	g skills to express their thoughts freely and fl	uently							
3.Learn strategies	for effective reading								
4.Write grammatic	ally correct sentences in general and academ	ic writing							
5. Develop technic	al writing skills like writing instructions, tra	nscoding etc.,							
Module:1 Lister	ning		8 hours						
Understanding Con	nversation								
Listening to Speec	hes								
Listening for Spec	fic Information	•							
Module:2 Speak	ing		4 hours						
Exchanging Inform	nation								
Describing Activit	ies, Events and Quantity	•							
Module:3 Read	ing		6 hours						
Identifying Inform	ation								
Inferring Meaning									
Interpreting text									
Module:4 Writin	ng: Sentence		8hours						
Basic Sentence Str	ucture								
Connectives									
Transformation of	Sentences								
Synthesis of Sente	nces								
Module:5 Writin	ng: Discourse		4hours						
Instructions									
Paragraph									
Transcoding									
	Тс	otal Lecture hou	irs: 30 hours						
1 ext Book(s)									
1. Reaston, Chi	ris, incresa Clementson, and Gillie C	unningnam. Fa	ce2face Upper						
Intermediate S	Sudem's BOOK. 2015, Cambridge University	F1888.							
Kelerence Books	Reference Books								

1	1 Chris Juzwiak .Stepping Stones: A guided approach to writing sentences and Paragraphs							
	(Second Edition), 2012, Library of Congress.							
2.	. Clifford A Whitcomb & Leslie E Whitcomb, Effective Interpersonal and Team							
	Communication Skills for Engineer	rs, 2013, John Wi	ley & Sons	, Inc., Hoboken: Ne	ew Jersey.			
3.	ArunPatil, Henk Eijkman &Ena	Bhattacharya,	New Med	ia Communication	skills for			
	Engineers and IT Professionals,20	12, IGI Global, H	ershey PA.					
4.	Judi Brownell, Listening: Attitudes	, Principles and S	<i>Skills</i> , 2016	, 5 th Edition, Routle	edge:USA			
5.	John Langan, Ten Steps to Impro-	ving College Rea	ding Skills	s, 2014, 6 th Edition	, Townsend			
	Press:USA							
6.	Redston, Chris, Theresa Clementso	on, and Gillie Cu	nningham.	Face2face Upper I	ntermediate			
	Teacher's Book. 2013, Cambridge	University Press.						
	Authors, book title, year of publication	tion, edition num	ber, press,	place				
Mo	de of Evaluation: CAT / Assignmen	t / Quiz / FAT / P	roject / Ser	ninar				
	List of Challe	enging Experime	ents (Indica	ative)				
1.	Familiarizing students to adjective	es through brainst	orming adj	ectives with all	2 hours			
	letters of the English alphabet and	asking them to a	dd an adjec	tive that starts				
	with the first letter of their name a	is a prefix.						
2.	2. Making students identify their peer who lack Pace, Clarity and Volume during							
	presentation and respond using Symbols.							
3.	Using Picture as a tool to enhance	learners speaking	g and writin	ng skills	2 hours			
4.	Using Music and Songs as tools t	o enhance pronun	ciation in t	he target	2 hours			
	language / Activities through VIT	Community Rad	io					
5.	Making students upload their Self	- introduction vid	eos in Vim	eo.com	4 hours			
6.	Brainstorming idiomatic expression	ons and making th	em use the	se in to their	4 hours			
	writings and day to day conversat	ion						
7.	Making students Narrate events by	y adding more dea	scriptive ad	ljectives and add	4 hours			
	flavor to their language / Activitie	es through VIT Co	ommunity H	Radio				
8	Identifying the root cause of stage	e fear in learners a	nd providii	ng remedies to	4 hours			
	make their presentation better							
9	Identifying common Spelling & S	entence errors in	Letter Writ	ing and other day	2 hours			
	to day conversations							
10.	Discussing FAQ's in interviews w	vith answers so the	at the learn	er gets a better	2 hours			
	insight in to interviews / Activitie	s through VIT Co	mmunity R	ladio				
			Total L	aboratory Hours	30 hours			
Mo	de of evaluation: Online Ouizzog De	recentation Dolo	nlav Grou	Discussions Assi	anmente			
Mir	ni Project		piay, Olouj	DISCUSSIONS, ASSI	giinents,			
Rec	Recommended by Board of Studies 22.07.2017							
Apr	proved by Academic Council	No 46	Date	24-8-2017				
- API	noved by meadenine counten	110. TO	Date	27-0-2017				

ENG5002		Professional and Communicatio	n Skills	L T P J C		
				0 0 2 0 1		
Pre-requisite		ENG5001		Syllabus version		
				1.1		
Course Obje	ctives	3.				
1. To enable s	studer	nts to develop effective Language and Comm	unication Skills			
2. To enhance	e stud	lents' Personal and Professional skills				
3. To equip the	3. To equip the students to create an active digital footprint					
Expected Co	urse	Outcome:				
1. Improv	ve inte	r-personal communication skills				
2. Develo	op pro	blem solving and negotiation skills				
3. Learn	the sty	les and mechanics of writing research reports				
4. Cultiva	ate bet	ter public speaking and presentation skills				
5. Apply	the ac	quired skills and excel in a professional environr	nent			
Module:1	Pers	onal Interaction		2hours		
Introducing Or	neself-	one's career goals				
Activity: SWC	OT An	alysis				
Module:2	Inter	rpersonal Interaction		2 hours		
Interpersonal C	Comm	unication with the team leader and colleagues at	the workplace			
Activity: Role	Plays/	Mime/Skit	_			
Module:3	Socia	al Interaction		2 hours		
Use of Social I	Media,	, Social Networking, gender challenges				
Activity: Creat	ting Li	nkedIn profile, blogs				
Module:4	Résu	ımé Writing		4 hours		
Identifying job	requi	rement and key skills				
Activity: Prepa	are an	Electronic Résumé				
Module:5	Inter	rview Skills		4 hours		
Placement/Job	Interv	view, Group Discussions				
Activity: Mocl	c Inter	view and mock group discussion				
Module:6	Repo	ort Writing		4 hours		
Language and	Mecha	anics of Writing				
Activity: Writi	ng a R	Report				
Module:7	Stud	y Skills: Note making		2hours		
Summarizing t	he rep	ort				
Activity: Abstr	ract, E	xecutive Summary, Synopsis				
Module:8	Inter	rpreting skills		2 hours		
Interpret data i	n table	es and graphs				
Activity: Trans	scodin	g				
Module:9	Pres	entation Skills		4 hours		
Oral Presentati	ion usi	ng Digital Tools				
Activity: Oral	presen	tation on the given topic using appropriate non-v	erbal cues			
Module:10	Prot	olem Solving Skills		4 hours		
Problem Solvin	ng & (Conflict Resolution				
Activity: Case	Analy	sis of a Challenging Scenario				
		Total Lecture hours:		30hours		
Text Book(s)						
1 Bhatnag	gar Ni	tin and Mamta Bhatnagar, Communicative E	nglish For			
Enginee	ers An	d Professionals, 2010, Dorling Kindersley (I	ndia) Pvt. Ltd.			

Reference Books								
1	Jon Kirkman and Christopher Turk, Effective Writing: Improving Scientific, Technical and							
	Business Communication, 2015, Routledge							
2	Diana Bairaktarova and Michele	Eodice, Creative	Ways of H	Knowing in Eng	gineering, 2017,			
	Springer International Publishing							
3	Clifford A Whitcomb & Les	slie E Whitcom	b, <i>Effecti</i>	ve Interperson	nal and Team			
	Communication Skills for Engine	ers, 2013, John W	iley & Sor	ns, Inc., Hoboke	en: New Jersey.			
4	ArunPatil, Henk Eijkman &En	a Bhattacharya,	New Mea	lia Communice	ation Skills for			
	Engineers and IT Professionals,2	012, IGI Global, H	Hershey PA	Α.				
Mod	e of Evaluation: CAT / Assignmen	t / Quiz / FAT / P	roject / Sei	ninar				
List	of Challenging Experiments (Inc	licative)						
1.	SWOT Analysis – Focus specially of	on describing two st	rengths and	two	2 hours			
	weaknesses							
2.	. Role Plays/Mime/Skit Workplace Situations							
3.	3. Use of Social Media – Create a LinkedIn Profile and also write a page or two on							
	areas of interest							
4.	Prepare an Electronic Résumé and u	pload the same in vi	meo		2 hours			
5.	Group discussion on latest topics				4 hours			
6	Report Writing – Real-time repor	ts			2 hours			
7	Writing an Abstract, Executive S	ummary on short s	cientific o	r research	4 hours			
	articles							
8	Transcoding – Interpret the given	graph, chart or di	agram		2 hours			
9	Oral presentation on the given top	oic using appropria	ate non-ve	rbal cues	4 hours			
10	Problem Solving Case Analysis of	a Challenging Scer	nario		4 hours			
		Т	otal Labo	ratory Hours	30 hours			
Mod	e of evaluation: : Online Quizzes, I	Presentation, Role	play, Grou	up Discussions	, Assignments,			
Mini Project								
Reco	Recommended by Board of Studies 22-07-2017							
App	roved by Academic Council	No. 47	Date	05-10-2017				

FRE5001		FRANCAIS FONCTION	NEL L T P J C					
Pre-requisi	te			Syllabus version				
Nil	• .•			1.0				
Course Ob	jectives							
The course	gives st	udents the necessary background to:						
I. Den	1. Demonstrate competence in reading, writing, and speaking basic French, including							
Knov	knowledge of vocabulary (related to profession, emotions, rood, workplace,							
spor	iovo pr	ies, classiform and family).	nt					
2. Atl	2. Achieve pronciency in French culture offended view point.							
Expected (OURSO	Autcome:						
The student	s will b	e able to						
1 Rem	ember	the daily life communicative situations via n	ersonal pronour	s emphatic				
pron	ouns, s	alutations, negations, interrogations etc.	ersonar pronoar	is, emphane				
2. Crea	ite com	municative skill effectively in French langua	ge via regular /	irregular verbs.				
3. Den	onstrat	e comprehension of the spoken / written lang	guage in translat	ting simple				
sente	ences.	· · · · · · · · · · · · · · · · · · ·	58	8 <u>F</u>				
4. Und	erstand	and demonstrate the comprehension of some	e particular new	range of unseen				
writ	ten mat	erials.	•	C				
5. Dem	nonstrat	e a clear understanding of the French culture	through the lar	guage studied.				
Module:1	Saluer	r, Se présenter, Etablir des contacts		3 hours				
Les Salutati	ons, Le	s nombres (1-100), Les jours de la semaine,	Les mois de l'a	année, Les Pronoms				
Sujets, Les	Pronor	ns Toniques, La conjugaison des verbes rég	guliers, La conj	ugaison des verbes				
irréguliers-	avoir /	être / aller / venir / faire etc.						
Module:2	Prése	nter quelqu'un, Chercher un(e)		3 hours				
	corre	spondant(e), Demander des nouvelles						
	a une	personne.						
La c	oniugai	son des verbes Pronon	ninaux I	a Négation				
L'interrogat	ion ave	c 'Est-ce are ou sans Est-ce are'	innaux, i	La Regation,				
Lintenogu	.1011 4 V C	S Est ce que ou suns Est ce que .						
Module:3	Situe	un obiet ou un lieu. Poser des questions		4 hours				
L'article (d	éfini/ i	ndéfini). Les prépositions (à/en/au/aux/sur/c	lans/avec etc.).	L'article contracté.				
Les heures	en fra	nçais, La Nationalité du Pays, L'adjectif	(La Couleur,	l'adjectif possessif,				
l'adjectif de	émonst	ratif/ l'adjectif interrogatif (quel/qu	elles/quelle/que	lles), L'accord des				
adjectifs ave	ec le no	m, L'interrogation avec Comment/ Combier	/ Où etc.,					
Module:4	Faire	des achats, Comprendre un texte court,		6 hours				
	Demander et indiquer le chemin.							
La traductio	on simp	le :(français-anglais / anglais –français)						
	-							
Module:5	Trouv	ver les questions, Répondre aux		5 hours				
	quest	ions générales en français.						

L'article Partitif, Mettez les phrases aux pluriels, Faites une phrase avec les mots donnés, Exprimez les phrases données au Masculin ou Féminin, Associez les phrases.

Module:6 Comment ecrire un passage

3 hours

4 hours

Décrivez :

La Famille /La Maison, /L'université /Les Loisirs/ La Vie quotidienne etc.

Module:7 Comment ecrire un dialogue

Dialogue:

- a) Réserver un billet de train
- b) Entre deux amis qui se rencontrent au café
- c) Parmi les membres de la famille
- d) Entre le client et le médecin

Module:8	Invited Talk: Native speakers	2 hours

			Total Lecture ho	ours: 3	0 hours		
Tex	kt Book(s)					
1.	Echo-1	, Méthode de français, J. Gi	rardet, J. Pécheur,	Publishe	r CLE Inter	mational, Paris 2010.	
2	Echo-1	, Cahier d'exercices, J. Gira	rdet, J. Pécheur, P	ublisher	CLE Intern	ational, Paris 2010.	
Ref	erence l	Books					
1.	CONN	EXIONS 1, Méthode de fra	nçais, Régine Mér	ieux, Yve	es Loiseau,l	Les Éditions Didier,	
	2004.						
2	CONN	EXIONS 1, Le cahier d'ex	ercices, Régine M	érieux, Y	ves Loiseau	ı, Les Éditions	
	Didier,	2004.					
3	ALTE	R EGO 1, Méthode de franc	ais, Annie Berthe	t, Catheri	ne Hugo, V	éronique M.	
	Kiziria	n, Béatrix Sampsonis, Mon	que Waendendrie	s, Hacher	tte livre 200)6.	
		-	-				
Mo	Mode of Evaluation: CAT / Assignment / Quiz / FAT						
Rec	Recommended by Board of Studies						
Approved by Academic Council No 41 Date 17-06-2016						16	

GER5001 Deutsch für Anfänger I							
Pre-requisite	NIL	Syllabus version					
		1.0					
Course Objectives	s:						
The course gives st	tudents the necessary background to:						
1. Enable stuc	lents to read and communicate in German in their day to da	ay life					
2. Become ind	ustry-ready						
3. Make them	understand the usage of grammar in the German Language.						
Expected Course	Outcome:						
The students will be	able to						
1. Create the b	asics of German language in their day to day life.						
2. Understand	the conjugation of different forms of regular/irregular ver	bs.					
3. Understand	the rule to identify the gender of the Nouns and apply arti	cles appropriately.					
4. Apply the C	German language skill in writing corresponding letters, E-M	Mails etc.					
5. Create the t	alent of translating passages from English-German and vio	e versa and To frame					
simple dial	ogues based on given situations.						
Module:1		3 hours					
Einleitung, Begrüs	ssungsformen, Landeskunde, Alphabet, Personalpronome	n, Verb Konjugation,					
Zahlen (1-100), W	-tragen, Aussagesätze, Nomen – Singular und Plural						
Lernziel:	adnie von Dautsch, Conus, Artikolwörter						
	idnis von Deutsch, Genus- Artikerworter						
Module:2		3 hours					
Konjugation der V	erben (regelmässig /unregelmässig) die Monate, die Woch	entage, Hobbys,					
Berufe, Jahreszeite	n, Artikel, Zahlen (Hundert bis eine Million), Ja-/Nein-Fr	age, Imperativ mit					
Sie							
Lernziel :							
Sätze schreiben, übe	r Hobbys erzählen, über Berufe sprechen usw.						
Module:3		4 hours					
Possessivpronome	n, Negation, Kasus- AkkusatitvundDativ (bestimmter,)	IndestimmterArtikel),					
Gotrönko	, Modalverben, Adjektive, Unrzeit, Prapositionen, Man	izeiten, Lebensmittei,					
Sätze mit Modalverh	ben. Verwendung von Artikel, über Länder und Sprachen sprech	ien, über eine Wohnung					
beschreiben.	beschreiben.						
Module:4		6 hours					
Übersetzungen : (I	Deutsch – Englisch / Englisch – Deutsch)						
Lernziel :							
Grammatik – Wortschatz – Übung							
	I						
Nodule:5		5 hours					
Leseverständnis,M	inamap machen,Korrespondenz- Briefe, Postkarten, E-Ma	.11					
Lernziei :							

Wo	ortschatz	bildung und aktiver Sprach	gebrauch						
Mo	odule:6							3 h	ours
Au	Aufsätze :								
Me	ine Univ	versität, Das Essen, mein Fro	eund oder meine	Freund	in, meine	e Fami	ilie, ein Fes	t in	
Der	utschland	d usw							
Mo	odule:7							4 ho	ours
Dia	aloge:								
	e) Gesp	präche mit Familienmitglieder	n, Am Bahnhof,						
	f) Gesp	präche beim Einkaufen ; in ein	em Supermarkt ; ir	n einer l	Buchhanc	llung ;			
	g) in ei	nem Hotel - an der Rezeption	;ein Termin beim /	Arzt.					
Tre	effen im	Cafe							
Mo	odule:8							2 ho	ours
Gue	est Lectu	ares/Native Speakers / Fein	nheiten der deuts	schen	Sprache,	Basis	information	über	die
deu	tschsprac	higen Länder			T				
			Total Lecture h	ours:	30 hou	irs			
Te	xt Book(s)							
1.	Studio	d A1 Deutsch als Fremdsp	orache, Hermann	Funk,	Christin	a Kuł	ın, Silke Do	emme	:
	2012								
Re	ference]	Books							
1	Netzwe	rk Deutsch als Fremdsprache	A1, Stefanie Dengl	er, Paul	Rusch, H	elen So	chmtiz, Tanja	a Siebe	er,
	2013								
2	Lagune	e,Hartmut Aufderstrasse, J	utta Müller, Thon	nas Sto	orz, 2012	•			
3	Deutsch	ne SprachlehrefürAUsländer, H	leinz Griesbach, Do	ora Sch	ulz, 2011				
4	Themer	nAktuell 1, HartmurtAufderstr	asse, Heiko Bock, N	Mechthi	ildGerdes	, Jutta	Müller und I	Helmu	t
	Müller,	2010							
	www.g	<u>pethe.de</u>							
	wirtsch	aftsdeutsch.de							
	hueber	.de, klett-sprachen.de							
	www.d	eutschtraning.org							
Mo	de of Ev	aluation: CAT / Assignmen	t / Quiz / FAT						
Red	commen	ded by Board of Studies							
Ap	proved b	y Academic Council	No. 41	Date	17-	-06-20	16		

STS500	01	Essentials of Business Etiqu	iettes	L T P J C		
				3 0 0 0 1		
Pre-requ	isite			Syllabus version		
Course Ob	jectives	•				
1. To d	levelop	the students' logical thinking skills				
2. To le	earn the	e strategies of solving quantitative ability pro	blems			
3. To e	enrich th	ne verbal ability of the students				
4. To e	enhance	critical thinking and innovative skills				
Expected C	Course	Outcome:				
• Enal	bling st	udents to use relevant aptitude and appropria	te language to e	xpress themselves		
• To c	ommuni	cate the message to the target audience clearly				
Module:1	Busin	ess Etiquette: Social and Cultural		9 hours		
	Etiqu	ette and Writing Company Blogs and				
	Interi	al Communications and Planning and				
	writi	ng press release and meeting notes				
Volue Monn	Cura	toma Language Tradition Duilding a blog Day	valoning brand m			
Assessing Co	ompetiti	on Open and objective Communication. Two ways	v dialogue Unde	essage, FAQS,		
audience Ide	entifving	Gathering Information Analysis Determining	Selecting plan	Progress check		
Types of plan	nning. V	Vrite a short, catchy headline. Get to the Point –s	ummarize vour su	biect in the first		
paragraph., E	Body - N	Aake it relevant to your audience,	j			
	2	•				
Module:2	Study	skills – Time management skills		3 hours		
Prioritization	, Procra	stination, Scheduling, Multitasking, Monitoring,	Working under p	pressure and adhering		
to deadlines						
Madular2	Duego	tation skills . Drongwing progentation		7 h auna		
Module:5	Prese	ntation skills – Preparing presentation	7 not			
	and C	reparing materials and Maintaining				
	and p	reparing visual alus and Deaning with				
	quest	lons				
10 Tips to r	renare	PowerPoint presentation Outlining the content	Passing the Fle	vator Test Blue sky		
thinking. Intr	roductio	n body and conclusion. Use of Font, Use of Co	lor. Strategic pres	sentation. Importance		
and types of	visual a	aids, Animation to captivate your audience, Des	sign of posters, S	etting out the ground		
rules, Dealin	rules, Dealing with interruptions, Staying in control of the questions, Handling difficult questions					
				P		
Module:4	Quan	titative Ability -L1 – Number properties		11 hours		
	and A	verages and Progressions and				
Perc		ntages and Ratios				
Number of f	factors,	Factorials, Remainder Theorem, Unit digit po	sition, Tens digit	t position, Averages,		
Weighted A	verage,	Arithmetic Progression, Geometric Progression	n, Harmonic Pro	gression, Increase &		
Decrease or s	Decrease or successive increase, Types of ratios and proportions					

Mo	dule:5	Reasoning Ability-L1 – A	Analytical Reason	ing	8 hours				
Dat	Data Arrangement(Linear and circular & Cross Variable Relationship), Blood Relations,								
Ord	Ordering/ranking/grouping, Puzzle test, Selection Decision table								
Mo	dule:6	Verbal Ability-L1 – Voca	abulary Building		7 hours				
~									
Sy	nonyms a	& Antonyms, One word substi	tutes, Word Pairs, S	pellings, I	lioms, Sentence completion,				
Ar	lalogies		Total Lastrum h		45 h a				
			Total Lecture no	ours:	45 hours				
Ref	ference	Books		~ • • • •					
1.	Kerry I	Patterson, Joseph Grenny, R	on McMillan, Al	Switzler(2	001) Crucial Conversations:				
	Tools f	or Talking When Stakes are	e High. Bangalore.	McGraw	-Hill Contemporary				
2.	Dale Ca	rnegie,(1936) How to Win Fr	iends and Influence	People. Ne	ew York. Gallery Books				
3.	Scott Pe	eck. M(1978) Road Less Trave	elled. New York Cit	y. M. Scot	Peck.				
4.	FACE(2	2016) Aptipedia Aptitude Enc	yclopedia. Delhi. W	iley public	ations				
5.	ETHNU	JS(2013) Aptimithra. Bangalo	re. McGraw-Hill Ec	lucation Pv	rt. Ltd.				
We	bsites:								
1.	www.cl	nalkstreet.com							
2.	www.sk	<u> cillsyouneed.com</u>							
3.	www.m	indtools.com							
4.	www.th	ebalance.com							
5.	5. www.eguru.ooo								
Mo	de of Ev	valuation: FAT, Assignmen	ts, Projects, Case	studies, R	ole plays,				
3 A	3 Assessments with Term End FAT (Computer Based Test)								
Rec	Recommended by Board of Studies 09/06/2017								
Ap	Approved by Academic Council No. 45 th AC Date 15/06/2017								

STS50	02	Preparing for Industry	7	L T P J C	
				3 0 0 0 1	
Pre-requ	isite			Syllabus version	
~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~				2.0	
Course Ob	jectives				
5. To c	levelop	the students' logical thinking skills	1.1		
$\begin{array}{c} 6. 101 \\ 7 T \end{array}$	earn the	e strategies of solving quantitative ability pro	blems		
/. loe	enrich tr	le verbal ability of the students			
<u>ð. 10 e</u>	ennance	crucal uninking and innovative skins			
Expected (Course	Outcome:			
• Enal	bling st	udents to simplify, evaluate, analyze and use	functions and e	xpressions to	
simu	ulate rea	I situations to be industry ready.			
Module:1	Interv	view skills – Types of interview and		3 hours	
	Techr	iques to face remote interviews and			
	Mock	Interview			
Structured a	and unst	ructured interview orientation, Closed quest	ions and hypoth	etical questions,	
Interviewer	s' persp	ective, Questions to ask/not ask during an in	terview, Video i	interview	
Recorded fe	edback	, Phone interview preparation, Tips to custor	nize preparation	for personal	
interview, P	ractice	rounds			
Modulo.2	Dogur	no skills – Dosumo Tomplato and Uso of		2 hours	
Wibuule.2	ncsui	r verbs and Types of resume and		2 11001 5	
	Custo	mizing resume			
Structure of	f a stan	dard resume. Content. color. font. Introduc	tion to Power v	erbs and Write up.	
Quiz on ty	pes of	resume, Frequent mistakes in customizing	resume, Layou	ut - Understanding	
different co	n mpany':	s requirement, Digitizing career portfolio		U	
Module:3	Emot	ional Intelligence - L1 – Transactional		12 hours	
	Analy	sis and Brain storming and			
	Psych	ometric Analysis and Rebus			
	Puzzl	es/Problem Solving			
Introduction	n, Con	tracting, ego states, Life positions, I	ndividual Brai	nstorming, Group	
Brainstormi	ing, Ste	pladder Technique, Brain writing, Crawfor	d's Slip writing	approach, Reverse	
brainstorming, Star bursting, Charlette procedure, Round robin brainstorming, Skill Tes					
Personality Test, More than one answer, Unique ways					
Modulo:4	Quan	titative Ability I 3 Permutation		1/ hours	
Com		inations and Probability and Geometry		14 110015	
	and m	nensuration and Trigonometry and			
	Logar	ithms and Functions and Ouadratic			
	Equat	tions and Set Theory			
L					

Counting, Grouping, Linear Arrangement, Circular Arrangements, Conditional Probability, Independent and Dependent Events, Properties of Polygon, 2D & 3D Figures, Area & Volumes, Heights and distances, Simple trigonometric functions, Introduction to logarithms, Basic rules of logarithms, Introduction to functions, Basic rules of functions, Understanding Quadratic Equations, Rules & probabilities of Quadratic Equations, Basic concepts of Venn Diagram

Module:5 Reasoning ability-L3 – Logical reasoning and							
Data Analysis and Interpretation							
Syl	logisms,	Binary logic, Sequential or	tput tracing, Crypt	o arithr	netic, Data Sufficiency, Data		
inte	erpretatio	on-Advanced, Interpretation	tables, pie charts &	& bar cł	nats		
Mo	dule:6	Verbal Ability-L3 – Com	prehension and		7 hours		
		Logic					
Rea	ading con	nprehension, Para Jumbles,	Critical Reasoning	g (a) Pre	emise and Conclusion, (b)		
Ass	sumption	& Inference, (c) Strengther	ning & Weakening	an Arg	ument		
			Total Lecture ho	urs:	45 hours		
Ref	ference 1	Books					
1.	Michae	el Farra and JIST Editors(20	11) Quick Resume	e & Cov	ver Letter Book: Write and Use an		
	Effecti	ve Resume in Just One Day	. Saint Paul, Minne	esota. Ji	st Works		
2.	Daniel	Flage Ph.D(2003) The Art	of Questioning: An	Introdu	uction to Critical Thinking.		
	Londor	n. Pearson					
3.	David	Allen(2002) Getting Thing	s done : The Art of	f Stress	-Free productivity. New York		
	City. P	enguin Books.					
4.	FACE(2016) Aptipedia Aptitude E	Encyclopedia.Delhi	. Wiley	publications		
5.	ETHN	US(2013) Aptimithra. Bang	alore. McGraw-Hi	ll Educa	ation Pvt. Ltd.		
We	ebsites:						
1.	www.cl	nalkstreet.com					
2.	www.sł	<u>tillsyouneed.com</u>					
3.	www.m	indtools.com					
4.	www.th	ebalance.com					
5.	www.eg	<u>guru.000</u>					
Mo	de of Ev	valuation: FAT, Assignmen	nts, Projects, Case s	studies,	Role plays,		
3 A	ssessme	nts with Term End FAT (Co	omputer Based Tes	st)			
Rec	commen	ded by Board of Studies	09/06/2017				
Ap	Approved by Academic Council No. 45 th AC Date 15/06/2017						

Programme Core

Course C	ode	Course Title	L	ΤP	J	С	
ECE504	41	EMBEDDED SYSTEM DESIGN	EMBEDDED SYSTEM DESIGN3000				
Pre-requi	isite	Nil	Sy	llabu	IS		
			Vei	sion	1.1		
Course Ob	inativa						
The course of	aimed a	• f					
1 Abil	itv to	understand comprehensively the technologies and techniqu	ies	unde	lvir	no in	
build	ling an	embedded solution to a wearable, mobile and portable system.	105	unue	1 y 11	15 111	
2. Anal	lyze UN	AL diagrams and advanced Modelling schemes for different use	cas	es.			
3. Und	erstand	the building process of embedded systems					
Expected C	Course	Outcome:					
The students	s will b	e able to					
1. Defi	ne an e	mbedded system and compare with general purpose system.					
2. App	reciate	the methods adapted for the development of a typical embedded	l sys	tem.			
3. Get 1	introdu	ced to RIOS and related mechanisms.					
4. Clas 5 Diff	siry typ erentiat	e the features of components and networks in embedded system	1 C				
6. Deve	elon rea	l-time working prototypes of different small-scale and medium	-sca	le em	bed	ded	
Syste	ems.						
7. App	rehend	the various concepts in Multi Tasking					
		` `					
Module:1	Intro	luction to Embedded System			5 ł	iours	
Embedded	system	processor, hardware unit, software embedded into a system	n, E	xamp	ole (of an	
embedded s	ystem,	Embedded Design life cycle, Layers of Embedded Systems.					
Malaz	T.I.				<u> </u>		
Module:2	Emp	added System Design Methodologies	1 T	МЛ	<u>5 r</u>	10urs	
Requiremen	System t Analy	i modenning [FSM, SysML, MARTE], UML as Design too	I, U	NIL	nota	ation,	
Requirement	n Anary	sis and Use case Wodening, Design Examples					
Module:3	Build	ing Process For Embedded Systems			4 ł	iours	
Preprocessin	ng, Cor	npiling, Cross Compiling, Linking, Locating, Compiler Driver,	Lin	ker M	lap	Files,	
Linker Scrip	ots and	scatter loading, Loading on the target, Embedded File System.				·	
Module:4	Syste	m design using general purpose			7 ł	iours	
	proce	ssor					
Microcontro	oller ar	chitectures (RISC, CISC), Embedded Memory, Strategic selection		i of j	roc	essor	
and memor	y, Mer	hory Devices and their Characteristics, Cache Memory and	var	ious	maj	pping	
techniques,	DMA.						
Module:5	Comr	oonent Interfacing & Networks			9 ł	ours	
Memory Interfacing I/O Device Interfacing Interrupt Controllers Networks for Embedded						edded	
systems- U	SB, PC	CI,PCI Express, UART, SPI, I2C, CAN, Wireless Applicat	ions	- B	lue	tooth,	
Zigbee,Wi-I	Fi.,6Lo	WPAN, Evolution of Internet of things (IoT).					
]	
Module:6	Opera	ating Systems			7 ł	iours	

Introduction to Operating Systems, Basic Features & Functions of an Operating System, Kernel & its Features [polled loop system, interrupt driven system, multi rate system], Processes/Task and its states, Process/Task Control Block, Threads, Scheduler, Dispatcher.

Mo	dule:7	Multi Tasking				6 hours	
Cor	Context Switching, Scheduling and various Scheduling algorithms, Inter-process Communication						
(Shared Memory, Mail Box, Message Queue), Inter Task Synchronization (Semaphore, Mutex),					(Semaphore, Mutex),		
Dea	ud Lock,	Priority Inversion (bo	unded and un	bounded), I	Priority Ceilin	g Protocol & Priority	
Inh	eritance	Protocol					
Mo	dule:8	Contemporary issues	•		2 hours		
						1	
			Total Lectu	are hours:	45 hours		
Tex	t Book(s)			·		
1.	Raj Ka	mal, "Embedded systems	s Architecture,	Programmi	ing and Design	n", Tata McGraw- Hill,	
	2016.						
2.	Wayne	Wolf "Computers as con	nponents: Princ	ciples of Em	nbedded Comp	uting System Design",	
	The Mo	organ Kaufmann Series in	n Computer Are	chitecture an	nd Design, 201	3.	
Ref	erence I	Books					
1.	Lyla B.	Das," Embedded System	ns an Integrated	l Approach'	", Pearson Edu	cation, 2013.	
2.	Shibu F	K V," Introduction to Em	bedded System	s", McGraw	v Hill Educatio	n(India) Private	
	Limited	l, 2014					
3.	Sriram	V Iyer, Pankaj Gupta	" Embedded 1	Real Time	Systems Prog	ramming", Tata	
	McGrav	w-Hill, 2012					
4.	Steve H	leath, "Embedded Systen	ns Design", ED	N Series, 2	013.		
Mo	de of E	valuation: Continuous A	ssessment Tes	st, Quiz, Di	igital Assignm	ent, Final Assessment	
Tes	t.						
Recommended by Board of Studies 12/09/2020							
App	proved b	y Academic Council	No. 59	Date	,	24/09/2020	

Course cod	e	Course Title		L T P J C		
ECE5042	2 Microcontroller Architecture and Organization 2 0 2 4 4					
Pre-requisi	Pre-requisite Nil Syllabus version:					
Course Obj	jectives	:				
The course i	is aimed	l at				
[1] Describi	ng the a	architecture of 8051 microcontroller and AR	M processor			
[2] Teaching	g the in	struction set of 8051 and ARM microcontrol	ler to efficien	t programs		
[3] Designir	ng syste	m in block level using microcontroller, mem	ory devices, l	ouses and other		
peripheral d	evices					
[4] Solving	real life	problem using microcontroller-based system	ns			
Expected C	ourse	Jutcome:				
At the end of	of the co	burse, the students will be able to				
[1] Describe	the arc	chitectures of processors				
[2] Develop	Assem	bly program applying Digital logic and math	nematics using	g 8051		
[3] Develop	Assem	bly Language Program ALP for ARM and A	RM peripher	als		
[4] Develop	ALP w	ith minimum instructions and memory.				
[5] Analyze	and eva	aluate the given program in terms of code siz	ze and comput	tational time		
[6] Design N	Microco	ntroller based system within realistic constra	aint like user s	specification,		
availability	of com	ponents etc				
[7] Solve rea	al life p	roblem and construct a complete system as a	i solution			
[8] Integrate		and a working model using the laboratory co	mponents and	IDE tools.		
Module:1	Intro	duction to Microcontrollers	2 nours			
Endion Va	essors Dia En	vs Microcontrollers; Classification – bits, 1	memory archi	itecture, ISA; Little		
Modulo:2		ulall. Microcontrollor	2 hours			
Architectu	<u> </u>	imers Interrupts Register Architecture (2 nours banks) PSW	register Memory		
architectur	e: Instr	uction set		register, wremory		
Module:3	<u>8051</u>	Programming and Interfaces	5 hours			
Programm	ing in C	C & Assembly for – Interrupts, Timers and I	Interfaces – P	ORTS, LED, ADC,		
SENSORS	, ĽCD,	DAC, Serial Communication.				
Module:4	ARM	Architecture	3 hours			
ARM Des	ign Ph	losophy; Overview of ARM architecture;	States [ARM	I, Thumb, Jazelle];		
Registers,	Modes;	Conditional Execution; Pipelining; Vector	Fables; Excep	tion handling.		
Module:5	ARM	Instruction Set	6 hours			
ARM Instru	iction-	data processing instructions, branch instruc	tions, load st	ore instructions, SWI		
instruction,	Loadin	g instructions, conditional Execution, Assem	bly Programn	ning.		
Module:6	Thur	nb Instruction Set	4 hours			
Thumb Ir	istructio	on-Thumb Registers, ARM Thumb interwor	rking, branch	instruction, data		
processin	g instr	uction, single/multiple load store instruct	tion, Stack 1	nstruction, SWI		
Instruction	n, Asse	moly Programming.	(hours			
Architectur	re of I I	COLE DASCU MICLOCONTONEL PC214X Memory Addressing IO ports Tim	o nours	Vatch Dog Timer		
PWM AD	C/DAC	L UART. Interrupts. Displays C programmi	ng.			
Module:8	Conte	mporary Issues	2 hours			
		Total Lecture Hours:	30 hours			

Text	Book(s)					
1. Ar	ndrew N.Sloss, Dominic Symes, Chris Wright, ARM Developer's Guide, 201	0, 1 st Edition,				
Elsevier, United States						
2. Kenneth Ayala, The 8051 Microcontroller & Embedded Systems Using Assembly and C, 2010,						
1st edition, Cengage Learning, United States						
Refe	rence Books					
1.Ste	ve Furber ARM System on Chip Architecture, 2010, 2 nd Edition, Addison Wes	sley,				
Unite	d States					
2. Te	chnical Reference Manual CORTEX M-3, ARM, 2010, United States					
Mode	e of Evaluation: CAT / Assignment / Quiz / FAT / Project / Seminar					
List	t of Challenging Experiments (Indicative)					
1.	Task-1: Calculator Application	7 hours				
	Sub task 1: Make the LCD interfaced to 8051					
1	Sub task 2: Get input from switch which is interfaced to 8051 and					
	display it on LCD					
	Sub task 3: Based on switch input, perform basic operation of a					
	Calculator					
2.	Task-2: Speed control of motor	7 hours				
	Sub task-1: Use timer and generate an exact time delay for Ton and					
1						
	Sub task-2: Use timer interrupt in generating the waveform					
	Sub tast-2: Controlling speed of a DC motor using Timer					
3	Task-3: Microcontroller based application	8 hours				
5.	Sub task-1: Interface Zighee with 8051	0 110013				
	Sub Task-1: Interface Ligbee with 8051					
	Sub Task 2: Interface GSM with 8051					
	Sub task-4: Based on KEY pressed in keypad transmit the key info					
	via Zigbee and make a motor to rotate, which is interfaced with 8051					
	Using GSM module send the status of motor[run/stop] to the user					
	Test 4. Sensor interfacing with ADM I DC2149	9 hours				
4.	Sub Took 1: Interfacing Will ARVI LPC2148	8 nours				
	Sub Task-1: Interface IR with LPC2148					
	Sub Task-2: Interface temperature sensor with LPC2148					
	Sub Task-3: Interface Bluetooth with LPC2148					
	L PC2148 via Bluetooth					
	Total Laboratory Hours	30 hours				
Tvn	ical Projects	20 110415				
<u>- JP</u>	1. Develop an ARM based waste management system. In this, the sensors					
	are placed in the common garbage bins placed at the public places.					
	When the garbage reaches the level of the sensor, then that indication					
	will be given to ARM Micro controller. The controller will give					
	indication to the driver of garbage collection truck as to which garbage					
	bin is completely filled and needs urgent attention. ARM 7 will give					
	indication by sending SMS using GSM technology.					

- 2. Design an ARM based automated patient monitoring system which continuously measures the patient parameters such as heart rate and rhythm, respiratory rate, blood pressure and many other parameters has become a common feature of the care of critically ill patients. When accurate and immediate decision-making is crucial for effective patient care, electronic monitors frequently are used to collect and display physiological data.
- 3. Implement a Digital Clock and Alarm using ARM microcontroller that needs a keypad to be interfaced with the following requirement. Key 1 to turn on alarm, Key 2 to enable alarm settings, Key 3 to enable time settings, Key 4 to change hour's settings, Key 5 to change minute settings, Key 6 to increment the time, Key 7 to decrement the time. The normal time and alarm time should be displayed using 2 X 16 LCD and a buzzer should be triggered once the normal time equal to alarm time.
- 4. Develop an ARM Micro controller-based precision agriculture which includes accessing real-time data about the conditions of the crops, soil and ambient air. Sensors in fields measure the moisture content and temperature of the soil and surrounding air.

Recommended by Board of Studies	27/02/2016		
Approved by Academic Council	No. 40^{th}	Date	18-03-2016

Course Cod	L	Т	P	J	С			
ECE5053	ELECTRONICS HARDWARE SYSTEM	ELECTRONICS HARDWARE SYSTEM DESIGN					4	
Pre-requisit								
Course Objectives:								
The course is aimed at								
[1] Emphasir	g students the significant role of FPGA in System	design and d	levelop	men	t.			
[2] Teaching	[2] Teaching the students to develop program using Hardware Descriptive Language and model							
digital logic combinational and sequential circuits.								
[3] Enabling the students acquire knowledge in Interfacing peripherals, Board Design, Packaging,								
PCB Design	PCB Design and Analysis							
[4] Motivating students to solve real life problem using FPGA based systems.								
Course Outo	comes (CO):							
At the end of	the course the student will be able to							
[1] Compreh	end the architecture of FPGA and design flow							
[2] Understan	nd Hardware Description Language							
[3] Design ar	nd develop combinational logic circuits using Veril	og and VHD	L prog	ram.				
[4] Design ar	nd develop sequential logic circuits using Verilog a	nd VHDL pr	ogram.					
[5] Interface	peripherals with FPGA.							
[6] Design th	e PCB							
[7] Design F	PGA based system							
[8] Compreh	end upcoming trends in FPGA.							
Module:1 Programmable Logic Devices & FPGAs 3 hours								
Introduction	n to FPGAs, FPGA technologies, FPGA Archite	ctures [Xilin	ix, Alte	era, 1	ACT	EL,		
LATTICE], FPGA Design Flow Prototyping with Xilinx FPGAs, FPGA based Testing.								
Module:2	Hardware Descriptive Language							
	(Verilog/VHDL)	3 hours						
Introduction, HDL Design flow, Language constructs -operators –Data types, Different								
architectures	(Structural, Behavioural, Dataflow)-Design examp	oles						
Module:3	Modeling of Combinational logic circuits	4 hours						
Half adder,	Full adder, 4-bit/8-bit binary adder, ALU design	, Multiplexe	r and I	De-m	ultip	lexe	r,	
Encoder, De	ecoder, Comparator, Ripple Carry Adder, Carry Lo	ok ahead ado	der.					
Module:4	Modeling of Sequential logic circuits	4 hours						
Flip Flops	-Realization of Shift Register -Realization of	of a Count	ter-Syn	chro	nous	ar	ıd	
Asynchrono	ous - BCD counter, Mealy and Moore State Ma	chines, Sequ	ience d	letec	tor,	FIFO),	
Memory De	sign, Serial Data Receiver, Serial to parallel data c	onverter.						
Module:5	Interfacing peripherals and Board Design	5 hours						
Interfacing	to 7 segment display, Stepper Motor, ADC and Se	ensors, FPGA	A System	m				
Architecture, Constraints – Logical – Electrical - Physical, Power distribution for FPGAs,								
Clock design, I/O buses.								
Module:6Introduction to Packaging &PCB Design4 hours								
Physical int	egration of circuits, packages, boards and full elect	ronic system	is - Pac	kage				
classificatio	ns (Through hole and SMDs) and packaging trends	s, Hierarchy	of Inter	con	necti	on		
Levels -Sig	nal integrity - The PCB Design Process - Defining	the Layout C	Cross Se	ectio	n - D)esig	'n	
Rules Checking - Working with Properties & Constraints- PCB Electrical Design Consideration -								
Design tips	for Placement / Fan-out and Wiring - Multi - Laye	r Design Issu	ies.					
Module:7	High Speed PCB design and Analysis	5 hours						

systems -Thermal interface material, Cooling mechanisms-System level design of electronic hardware for automotive applications -System level testing and validation of automotive electronics systems for reliability. Layout constraints for FPGAs, FPGA-based PCB schematics. Module:8 Contemporary issues: 2 hours Total Lecture hours: 30 hrs Text Book(s) 1. Simon Monk, Make Your Own PCBs with EAGLE: From Schematic Designs to Finished Boards, 2014, First Edition, McGraw Hill Education, India. 2. Wayne Wolf, FPGA-based System Design, 2011, Re-Print, Prentice Hall, India Reference Books 1. Clyde Coombs, Printed Circuits Handbook, 2011, Sixth Edition, McGraw Hill Professional, USA 2. Ian Grout, Digital Systems, Design with FPGAs and CPLDs, 2012, Re-Print, Newness, UK. 3. Ronald R. Sass and Andrew Schmidt, Embedded Systems Design with Platform FPGAs: Principles and Practices, 2010, First Edition, Morgan Kaufman Publishers, USA. Mode of Evaluation: Continuous Assessment Test, Quiz, Digital Assignment, Final Assessment Test. List of Challenging Experiments (Indicative)					
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Module:8 Contemporary issues: 2 hours Total Lecture hours: 30 hrs Total Lecture hours: 40 hrs Book(s) 1. Clyde Coombs, Prist Edition, McGraw Hill Education, India. 1. Clyde Coombs, Printed Circuits Handbook, 2011, Sixth Edition, McGraw Hill Professional, USA 2. Ian Grout, Digital Systems, Design with FPGAs and CPLDs, 2012, Re-Print, Newness, UK. 3. Ronald R. Sass and Andrew Schmidt, Embedded Systems Design with Platform FPGAs: Principles and Practices, 2010, First Edition, M					
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 Boards, 2014, First Edition, McGraw Hill Education, India. 2. Wayne Wolf, FPGA-based System Design, 2011, Re-Print, Prentice Hall, India Reference Books Clyde Coombs, Printed Circuits Handbook, 2011, Sixth Edition, McGraw Hill Professional, USA Ian Grout, Digital Systems, Design with FPGAs and CPLDs, 2012, Re-Print, Newness, UK. Ronald R. Sass and Andrew Schmidt, Embedded Systems Design with Platform FPGAs: Principles and Practices, 2010, First Edition, Morgan Kaufman Publishers, USA. Mode of Evaluation: Continuous Assessment Test, Quiz, Digital Assignment, Final Assessment Test. 					
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 Reference Books Clyde Coombs, Printed Circuits Handbook, 2011, Sixth Edition, McGraw Hill Professional, USA Ian Grout, Digital Systems, Design with FPGAs and CPLDs, 2012, Re-Print, Newness, UK. Ronald R. Sass and Andrew Schmidt, Embedded Systems Design with Platform FPGAs: Principles and Practices, 2010, First Edition, Morgan Kaufman Publishers, USA. Mode of Evaluation: Continuous Assessment Test, Quiz, Digital Assignment, Final Assessment Test. List of Challenging Experiments (Indicative) 					
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USA 2. Ian Grout, Digital Systems, Design with FPGAs and CPLDs, 2012, Re-Print, Newness, UK. 3. Ronald R. Sass and Andrew Schmidt, Embedded Systems Design with Platform FPGAs: Principles and Practices, 2010, First Edition, Morgan Kaufman Publishers, USA. Mode of Evaluation: Continuous Assessment Test, Quiz, Digital Assignment, Final Assessment Test. List of Challenging Experiments (Indicative)					
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 3. Ronald R. Sass and Andrew Schmidt, Embedded Systems Design with Platform FPGAs: Principles and Practices, 2010, First Edition, Morgan Kaufman Publishers, USA. Mode of Evaluation: Continuous Assessment Test, Quiz, Digital Assignment, Final Assessment Test. List of Challenging Experiments (Indicative) 					
FPGAs: Principles and Practices, 2010, First Edition, Morgan Kaufman Publishers, USA. Mode of Evaluation: Continuous Assessment Test, Quiz, Digital Assignment, Final Assessment Test. List of Challenging Experiments (Indicative)					
Publishers, USA. Mode of Evaluation: Continuous Assessment Test, Quiz, Digital Assignment, Final Assessment Test. List of Challenging Experiments (Indicative)					
Mode of Evaluation: Continuous Assessment Test, Quiz, Digital Assignment, Final Assessment Test.					
Assessment Test.					
List of Challenging Experiments (Indicative)					
List of Chanenging Experiments (indicative)					
1.Task 1: Combination Logic:-8 hours					
Design a 16-bit microprocessor that is capable of performing both logical					
and arithmetic operation.					
2.Task 2: Sequential Logic:-8 hours					
Design a controller for vending machine which sells candy bars for Rs 5, 10					
and 20.					
3.Task 3: Peripheral Interfacing:-8 hours					
Design a car speed monitor using the following components (a) 7 segment					
display (b) LEDs (c) Switches for speed selection and (d) Buzzer. The cars					
electronic speedometer provides a clock signal whose frequency is					
proportional to the speed. To check the functioning of the design use function					
generator to provide the speedometer clock.					
4. Task 4:PCB Design:- 6 hours					
Design a PCB for a circuit with a mixture of analog and digital parts, multiple					
power planes, and a single Ground plane split into analog and digital sections					
that have a common reference point using open source tool.					
Total Laboratory Hours : 30 Hours					
Mode of Evaluation: Continuous Assessment Test, Final Assessment Test					
Typical Projects:					

- 1. Design face recognition based Authenticated Door Opening System using FPGA. Database consisting of authorised persons faces should be created and the same should be compared with the real time camera input faces such that, if face matching happens then the door actuator needs to be triggered to open the door.
- 2. FPGA Implementation of Digital Clock and Alarm needs a keypad to be interfaced with the following requirement. Key 1 to turn on alarm, Key 2 to enable alarm settings, Key 3 to enable time settings, Key 4 to change hour's settings, Key 5 to change minute settings, Key 6 to increment the time and Key 7 to decrement the time. The normal time and alarm time should be displayed using 2 X 16 LCD and a buzzer should be triggered once the normal time equal to alarm time.
- 3. Design a GCD (Greatest Common divider) processor in FPGA. Use finite state machine approach of modelling the processor and generate the structure of Controller and Data path. The input should be given through the keypad which is to be interfaced with FPGA and the results should be serially transmitted to the Personal Computer through UART (Universal Asynchronous Receiver Transmitter) communication protocol.
- 4. Design a PCB of 3.3V/5V Power Supply and GSM Module. Individual switches need to be included to ON/OFF the individual Power Supply. The power supply and GSM schematic, top layer, bottom layer, top silk, top mask, top preview, bottom preview, bottom mask, drill file should be generated and captured during the design phase.

Mode of Evaluation: Project Reviews I, II, III

Approved by Academic Council : No. 40

Course code	Course Title		L	T	P	J	С
ECE5043	EMBEDDED PROGRAMMING	r J	3	0	2	0	4
Pre-requisite	None		Syllabus	ve	ersi	on	

Course Objectives :

The course is aimed

- 1. To acquaint students with fundamentals of C
- 2. To familiarize the students with data structures
- 3. To introduce the students with SHELL programming and Linux
- 4. To Implement the Device drivers in LINUX environment

Expected Course Outcome :

At the end of the course the students will be able to

- 1. Comprehend the fundamentals of C
- 2. Comprehend the Data structures
- 3. Comprehend the basics of Linux
- 4. Showcase the skill, knowledge and ability of SHELL programming.
- 5. Exhibit the working knowledge of basic Embedded Linux
- 6. Comprehend the concepts of Kernel module Programming
- 7. Write Device driver programs
- 8. Have hands on experience in using state-of- art hardware and software tools

Module:1 C Language

Basic concepts of C, Embedded C Vs C, Embedded programming aspects with respect to firmware and OS Functions, Arrays, pointers, structures and Inputs/Outputs.

7 hours

6 hours

6 hours

7 hours

6 hours

Module:2 Data structures of kernel programming

Linked list, Single linked list, Double linked list and Queues.

Module:3	Linux	

Command prompt, X windows basics, Navigating file system, finding files, working with folders, reading files text editing in Linux, Compression and archiving tools, Basic shell commands, File Management, I/O Handling, File Locking.

Module:4 Shell Programming

Processes, giving more than one command at a time, prioritizing and killing processes, Scheduling Commands, pipes and redirection, regular expression, pattern matching, Scripting using for while, if and other commands.

Module:5	Embedded Li	nux							6 hours
Linux Basi	cs, Booting pi	rocess, make	files,	using	SD ca	ard and	reader to	transfer	programs,
T 4 1 4		4 11	A DI 1	1 '	1 '		.1. 1	• 4 11•	- <u>1</u>

Introduction to LINUX system calls, API's, device drivers, compiling and installing a device driver.

Module:6 Kernel Module Programming

Compiling kernel, Configuring Kernel and compilation, Kernel code, browsers.-Static linking, dynamic linking of modules, User space, kernel space concepts, Writing simple modules – Writing, Make-files for modules.

Мо	dule:7	Device Driver concepts		5 hours
Dr	iver cor	ncepts, Block & character driver distinction, Low level drivers, OS	5 drive	ers etc, Writing
ch	aracter o	drivers, Device major, minor number.		
Mo	dule:8	Contemporary issues:		2 hours
		· · · · · · · · · · · · · · · · · · ·		
		Total Lecture hours: 45 hours		
Tex	t Books	S		
1.	Neil M	lathew, Richard stones, Beginning Linux Programming, 2012 reprin	nt, Wr	OX —
	Wiley	Publishing, USA.		
2.	Eric F	oster Johnson, John C. Welch, Micah Anderson, Beginning she	ell sci	ripting, 2012,
	reprint	, Wrox – Wiley Publishing, USA		
Ref	erence	Books		T 1 11 1
3.	Derek Linux,	Molloy, Exploring Beagle Bone: Tools and Techniques for Buildin 2015, 1 st Edition, Wiley Publications, USA	g with	h Embedded
Мо	de of E	valuation: CAT / Assignment / Quiz / FAT / Project / Seminar		
		List of Challenging Exp	erime	ents (Indicative)
1.	Task1:	C programming		6 hours
	•	Implement a binary tree sorting		
	•	Implement a dice throw game		
	•	Implement a command line argument based application of automa	tion	
2.	Task2:	Implementation of data structure for an application		6 hours
		Write a SortedMerge() function that takes two lists, each of white	ich is	
		sorted in increasing order, and merges the two together into on	e list	
		which is in increasing order. SortedMerge() should return the new	v list.	
		The new list should be made by splicing together the nodes of the	e first	
		two lists.		
3.	Task3:	Shell Programming		6 hours
	Develo	opment of inventory management system using Shell scripting wit	h the	
	follow	ing features		
	•	User may add/update/delete inventory.		
	•	User may add/update inventory details.		
	•	Details include cost, quantity and description.		
	•	Includes forms for inventory inwards and outwards.		
	•	User may create sub-inventories.		
	•	An interactive user interface.		
	•	A flexible inventory management system.		
4	Task4:	Build process for an embedded board		6 hours
		Build a kernel for a Beagle Bone Black (BBB) board and board	bring	
_		up, kernel module program on an embedded board		
5. T	Task5:	Device driver programming –Implementation of Device Driver		6 hours
Γot	al Laboi	ratory Hours		30 hours

Mode of evaluation: Continuous Lab Assessment								
Recommended by Board of Studies	12/09/2020							
Approved by Academic Council	No. 59 th	Date	24/09/2020					
Course Code	e Course Title		L	Т	Р	J	С	
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ECE5054	REAL TIME OPERATING SYST	EMS	3	0	2	0	4	
Pre-requisite	e Nil Sy	llabus Version	1 :1.1					
Course Object	Course Objectives:							
The course is aimed at								
[1]Introducing	g the students about Operating Systems and a	equainting stu	ident	s to	Rea	ıl Ti	me	
Operating S	Systems							
[2]Teaching t	he students about Task Management and Enab	oling students	to u	nders	stand	RT	OS	
Scheduling								
[3]Introducing	g the students about interprocess communication a	and Memory M	anag	eme	nt			
Course Outco	omes (CO):							
At the end of	the course the will should be able to							
[1]Compreher	nd the basic components of an operating system							
[2] Learn abou	it the basics of real-time concepts							
[3]Acquire kn	owledge about task management							
[4]Acquaint w	vith RTOS scheduling							
[5]Learn abou	t IPC synchronization							
[6]Learn abou	t IPC data exchange							
[7]Perform me	emory management in RTOS							
[8]Apply the l	knowledge for developing practical applications o	f modern real-	time	syste	ems.			
Module:1	Introduction to Operating Systems	6 hours						
Layers of O	perating Systems, Operating systems functions, S	System Boot u	p - E	BIOS	& I	Boot		
Process, Ker	nel – Monolithic and Microkernel	-	_					
Module:2	Real Time Operating Systems	7 hours						
Tradeoffs for	RTOS, POSIX							
Module:3	Task Management	7 hours						
Process and T	hreads, Process Control Block, Process Attributes	, POSIX Threa	ıds.					
Module:4	RTOS Scheduling	7 hours						
Priority based	scheduling, Rate-Monotonic scheduling, Earliest	Deadline first	sche	dulir	ıg,			
Linux RT sch	eduler.				-			
Module:5	IPC - Synchronization	7 hours						
IPC, Race con	ditions and critical sections, Signals, Atomic oper	rations, Semap	hore,	Mu	tex,			
Spinlock, Pric	rity Inversion and Priority ceiling.	1			,			
Module:6	IPC – Data Exchange	7 hours						
Shared memor	ry, FIFO, Messages and Mailbox, Circular and sw	inging buffers	, RPO	2				
Module:7	Memory Management	2 hours	<u>.</u>					
Memory Ma	nagement, shared memory							
Module:8	Contemporary issues:	2 hours						
		Total L	ectu	re h	ours	: 45	hrs	
Text Book(s								
1. Herma	K., Real Time Systems, Design for distributed En	nbedded Applic	catio	ns, 20	011,	2^{nd}		
edition	, Springer, USA.							
2 Tananh	Andrew Madam Onerstine Systems 2015	Ath ad Dearse	D					

2. Tanenbaum, Andrew, Modern Operating Systems, 2015, 4th ed.,, Pearson Prentice Hall, USA

Refe	Reference Books							
1.	1. Ivan CibrarioBertolotti, Politecnico di Torino and Gabriele Manduchi, Real-Time							
	Embedded Systems: Open-Source Operating Systems Perspective, 2012, 1 st ed.,							
	CRC Press, USA.							
2.	Lyla B. Das, Embedded Systems an Integrated Approach, 2012, 1 st ed., Pearson	Education,						
	India.							
Mod	e of Evaluation: Continuous Assessment Test, Quiz, Digital Assignment,							
Chal	lenging Experiments, Final Assessment Test.							
List	of Challenging Experiments (Indicative)	I						
1.	Write a C code for a simple calculator $(+, -, *, /)$ using functional pointer as	6 hours						
	argument in a function							
	int add (int x, int y)							
	int sub (int x, int y)							
	int mul (int x, int y)							
	int div (int x, int y)							
	int (*mathop)(int, int)							
	int domath(int (*mathop)(int , int), int x, int y)							
2.	Write a program to create multiple threads carrying out different functions.	6 hours						
	Thread 1: Accepting a string from the user.							
	Thread 2: Display the string in upper case.							
	Thread 3: Count the number of vowels in the string							
	Thread 4: Count the number of special characters in the string.							
3.	Write a program to create three threads, which are implemented using	6 hours						
	function pointers. First thread is for getting a list of numbers from the							
	keyboard, second thread is helpful to extract the ODD and EVEN list from							
	the given list, and the third one is used to arrange the ODD and EVEN list of							
	numbers in an order. Use Mutex semaphore.							
	Note:							
	First Thread for getting input data from keyboard.							
	Second Thread to identify the ODD and EVEN list							
	Third Thread to get descending ordered ODD list							
	Fourth Thread to get ascending ordered EVEN list							
	Input data: 56, 23, 12, 64, 87, 02, 45, 88, 35, 67							
4.	Write a Vx Works code for the given scenario. Also identify the proper	6 hours						
	mechanism to avoid this problem.							



Programme Elective

Course Code Course Title L T P J C							
ECE603	36	IN-VEHICLE NETWORK	ING	3 0 0 0 3			
Pre-requi	isite	Nil		Syllabus Version 1.2			
Course Obj		S:					
I ne course a	imed al	l udants a working knowledge of in vehicle net	vork systems				
2 Givin	no an e	xposure to aspects of design development apr	lication and perform	ance issues			
	ciated v	with in vehicle networking systems.	meanon and perform	lance issues			
3. Illust	trating	concepts of sensor data capture, storage and ex	change of data to acc	cess remote			
servi	ces		C				
Expected C	ourse	Outcome:					
The students	s will b	e able to					
1. Knov	w the ne	eed for In Vehicle Networking and the basics of	of data communication	on and			
netw	orking	concepts.					
2. Com	prehen	d protocols like CAN used in automotive appli	cations.				
3. Have		aza	AN open, Device N	iei, ITCAN			
4 Unde	erstand	the working mechanism of LIN protocol					
5. Get a	in over	view of MOST protocol used in automotive for	r multimedia applica	tions.			
6. Com	prehen	d protocols like FlexRay used in automotive fo	r fault tolerant applie	cations.			
7. Com	prehen	d the general protocols and their usage in autor	notive sector				
Module:1	Conce	epts of In-vehicle networking	6 hours				
Overview of	Data c	ommunication and networking-need for In-Ve	hicle networking-lay	yers of OSI			
reference mo	odel-mi	altiplexing and de-multiplexing concepts-vehic	cle buses.				
			0.1	1			
Module:2	Netw	orks and protocols	8 hours	fammata 1::4			
CAN protoco	ol: prin	ciples of data exchange-real time data transmis	ssion-message frame	bus access			
physical lave	r stand	and synchronization-data rate and bus length	-network topology-	bus access—			
physical laye							
Module:3	CAN	higher laver protocol	6 hours				
Introduction	to CAN	N open – Device net–TTCAN–SAEJ1939–over	view of CAN open a	nd applications in			
transportatio	n electr	onics–CAN open standards).	in or or or open a				
1		1					
Module:4	LIN	protocol	5 hours				
LIN standard	l overv	iew – applications – LIN communication conc	ept message frame-d	levelopment flow.			
Module:5	MOS	Γ	5 hours				
MOST overv	view-da	ata rates-data types-topology -application area	as.				
Module:6	FlexR	lay	6 hours				
Flex Ray int	roductio	on-network topology-ECU sand bus interfaces	s-controller host inte	rtace and protocol			
Pay schodul	ing me	searce processing, welcoup/startup, application	bcessing-coding/dec	ouing unit-Flex			
Ray scheuuli	ing-me	ssage processing— wakeup/startup-application					

Mo	dule:7	General purpose prot	tocols		7 hours			
GS	M- WiFi	 Bluetooth and NFC Imp 	lementation –E	thernet, TCI	P, UDP, IP.			
Mo	dule:8	Contemporary issues	:		2 hours			
					ſ			
			Total Lectu	ire hours:	45 hours			
Tex	<mark>xt Book</mark> (s)						
1.	Domini	que Paret, Multiplexed Ne	etworks for Emb	bedded Syste	ems CAN, LIN	, FlexRay, Safe by-		
	Wire, 2	014, 1 st edition, Wiley, Ur	ited States.					
Ref	ference I	Books						
1.	Chung	Ming Huang, YuhShyan C	Chen, Telematic	s Communic	cation Technol	ogies and		
	Vehicu	lar Networks: Wireless Ar	chitectures and	Application	, 2010, 1^{st} edit	ion,		
	Informa	tion Science Reference, U	Inited States.		th			
2.	Ronald	K Jurgen, Distributed Aut	comotive Embed	lded System	s, 2010, 4 th Ec	lition, SAE International,		
	United	States.				nd		
3.	Richard	l Zurawski, Industrial Con	nmunication Te	chnology Ha	andbook, 2015	, 2 nd Edition, CRC press,		
	United	States.						
4.	Konrad	Reif, Automotive Mechat	ronics: Automo	tive Networ	king, Driving	Stability Systems		
	Electron	nics, 2015, 2 nd Edition, Sp	ringer, United S	States.				
Mo	de of E	valuation: Continuous A	ssessment Tes	st, Quiz, Di	igital Assignn	nent, Final Assessment		
Tes	st.							
Rec	commend	led by Board of Studies		12/09/202	0			
Ap	proved b	y Academic Council	No. 59 th	Date		24-09-2020		

Course Code Course Title L T P J							
ECE6042 WIRELESS AND MOBILE COMMUNICATIONS 3 0						3	
Pre-requisite	Nil		Sy	llabu	IS 1 1		
			ve	rsion	1.1		
Course Obiecti	ves:						
The course aime	d at						
1. To know	about wireless mobile communication system	n & related issues, an	nd				
2. To keep	abreast of the future of mobile communication	1					
Expected Cours	se Outcome:						
The students will	l be able to						
1. Get intro	duced Cellular Mobile Communication system	ms					
2. Understa	nd and solve telecommunication design issues	s using cellular and t	runk	ting th	1001	ſy.	
3. Analyze	the effect of multipath channels and suggest a	suitable model for i	ndo	or or o	outo	loor	
applicati	ons.	in mahila aammunia	otio				
4. Demonst	the Channel coding for Mobile Padio	in mobile communic	allo	n.			
6 Interpret	the Modulation techniques for Mobile Radio						
7. Get intro	duced to Advanced Communication Systems	and Wireless Standa	rds				
Module:1 Ce	lular Mobile Systems	4 hours					
Cellular Mobile	Communication Evolution - Types of mobile	wireless services/sy	/ster	ns –	lG	& 2G	
Mobile Commu	nication Technology						
Module:2 Ce	llular Concept	7 hours					
Cellular concep	t – Frequency reuse – Channel assignm	ent strategies – Ha	ndo	ff stra	ateg	;ies –	
Interference & s	ystem capacity – Trunking & Grade of servi	ce – Improving cove	erag	e and	caj	pacity	
in cellular system	n.						
Madada 2 Ma		0.1					
Erros Spaces Drom	Dile Radio Propagation	9 nours	4 D	aflaat	ion	(Two	
Pree Space Prop	agation Model – Basic Propagation mechanis	n – I wo Kay Groun al Hata Model – Ji	u K ndov	or Dro	ion	(1wo	
Model: Attenuat	ion Factor Model	= $=$ $=$ $=$ $=$ $=$ $=$	nuo	ЛГЦ	pag	zation	
Widden Attendat							
Module:4 Sn	all Scale Propagation models	4 hours					
Parameters of r	nobile multipath channels – Types of small	scale fading – Fad	ing	effec	ts d	ue to	
Multipath time of	elay spread and Doppler spread		8	•			
1							
Module:5 Inf	ormation Theory and Coding	6 hours					
Information and	entropy - Coding of memoryless sources	: Shannon-Fano / H	Huff	man	cod	ling -	
Sources with n	nemory: Markov model - Source Coding:	Linear and non-li	near	qua	ntis	ation,	
companding -	Channel Coding: Convolutional coding, Viter	oi decoding, LBC, Tu	ırbo	Code	es.		
Module:6 Mu	Itiplexing & Modulation Schemes	6 hours			<u></u>		
FDMA, TDMA,	CDMA, QPSK, WCDMA, OFDM/OFDMA	, MC CDMA and SC	C FE	РМА,	CP	-	
OFDM and DFI	-S-UFD (16QAM, 64QAM, 256QAM)						

Mod	dule:7	Advanced Communic Wireless Standards	ation Systems	and	7 hours			
3G,	4G and	d 5G and beyond wirel	ess standards	- WLAN	Architecture de	esign and WIMAX –		
VAN	NETS					-		
Mod	dule:8	Contemporary issues	:		2 hours			
			Total Lectu	ire hours:	45 hours			
Tex	t Book(s)						
1.	Randy	L. Haupt, Wireless Comr	nunications Sy	stems: An I	ntroduction, Wi	iley-IEEE Press,		
	January	2020.	2			•		
2.	T.S.Ra	opaport, Wireless Comm	unication -Prin	ciple and Pi	actice, Prentice	Hall, 2010.		
Refe	erence l	Books		•				
1.	W.C.Y	Lee, Wireless and Cellul	ar Communica	tion, McGr	aw Hill, 2006			
2.	Schiller	, Mobile Communication	ns; Pearson Edu	acation Asia	a Ltd., 2008			
Mod	le of E	valuation: Continuous A	ssessment Tes	t, Quiz, D	igital Assignme	ent, Final Assessment		
Test					0 0			
Reco	ommend	led by Board of Studies		12/09/202	0			
App	roved b	y Academic Council	No. 59 th	Date	24/09/2020			

Course Code Course Title L T P J C									
ECE604	43	ADVANCED PROCESSORS AND ITS AP	PLICATIONS	2 0 0 4 3					
Pre-requi	isite	Nil	Syl	labus Version 1.1					
~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~									
Course Obj	jective	5:							
The course i	The course is aimed at								
I. Prov	'iding a	complete understanding of the ARM Cortex arc	chitecture.						
2. Impa	arting ti	he knowledge of programming ARM Cortex arcl	hitecture.	anala and					
3. Prov	laing K	nowledge on programmable DSPs Architecture,	, On-chip Peripi	herals and					
Eveneeted C	lourgo	Set.							
Expected C	ourse	outcome:							
1 I L cor	s WIII D	e able lo	ЛЛ						
1. Leal	II life a	Diffecture and instruction set of ARM Cortex M	14.						
2. Flog	alon an	plications based on Timers, DWM and ADC with	h ADM cortax	N T A					
J. Deve	orstand	and program the various communication modul	$\lim_{N \to \infty} ARM Contex$	1 1 1 1 1 1 1 1 1 1					
4. Ond	uire kn	and program the various communication modul	les of ARM Col	ICA 1914.					
6 Com	nrehen	ad programming of ARM 64 bit architecture							
0. Com 7 Dem	onstrat	te their ability to program the DSP processor for	signal processi	ng applications					
8 Desi	on ann	lication for various social relevant and real time	issues	ng apprications.					
0. Desi	<u>Sn upp</u>	neuton for various social felevant and fear time.	155405.						
Module:1	ARM	architecture and Cortex – M series 4 h	hours						
Introduction	to the	ARM Cortex M4 and its targeted application	ns ARM Corte	x M4 architecture					
address spa	ice. on	- chip peripherals (analog and digital) Regis	ster sets, addre	essing modes and					
instruction s	set basi	cs.							
Module:2	Micr	ocontroller Programming 6 h	hours						
ARM Corte	ex M4:	: I/O pin multiplexing, pull up/down registers,	GPIO control,	Memory Mapped					
Peripherals,	progr	amming System registers. Introduction to In	nterrupts, Inter	rupt vector table,					
interrupt pro	ogramn	ning.							
Module:3	Time	rs, PWM and Mixed Signals Processing 4 h	nours						
Timer, Basi	c Time	er, Real Time Clock (RTC), Timing generation	and measurem	ents, ADC. PWM					
Module & C	Quadrat	ure Encoder Interface (QEI).							
Module:4	Com	munication protocols and Interfacing 4 h	nours						
	with e	external devices							
12C protoco	I, SPI p	protocol, USB & UART protocol. Implementing	; and programm	ing I2C, SPI, USB					
& UART in	terface								
	4 70 7 7								
Module:5	AKM	Cortex A Architecture 4 h DM://2 A ADM://2 A Manuar M 4 h	10Urs	Madal C 1					
and Branch	n to A	KIVIVO-A, AKIVIVO-A Memory Management, Alton Synchronization and Cache coherency	KIVIV8-A Memo	bry Model, Caches					
		and Cache concretely.							
Module 6	Softw	are Engineers guide to ARM Cortex 64 2 h	ours						
mouule.0	hit ar	chitecture	IVII D						
Booting P	Power N	Management, Virtualization, Security Debugging	 σ.						

Mo	dule:7	DSP Processors	4 hours							
Arc	Architecture of TMS320CXX Processor – Addressing modes – Assembly language Instructions –									
Assembler directives, Pipeline structure, On-chip Peripherals – Block Diagram of DSP starter kit										
(DS	5K) – So	ftware Tools, DSK on-board peripherals, - Code Co	omposer Studio	o – Support Files -						
App	plication	Programs for processing real time signals.								
Mo	dule:8	Contemporary issues:	2 hours							
		Total Lecture hours:	30 hours							
Tex	kt Book(s)								
1.	Joseph	Yiu, "The Definitive Guide to ARM Cortex-M3 and	d Cortex-M4 P	Processors",						
	2013, 3	rd Edition, Newnes ,UK.								
2.	ARM C	Cortex-A Series Programmer's Guide for ARMv8-A	Version: 1.0,	2015,						
	ARM,	United States.								
3.	James A	A Langbridge, "Professional Embedded ARM Deve	lopment", 201	4,1st						
	Edition	, John Wiley Sons & Inc., United States.								
4.	Jonatha	in W. Valvono "Introduction to ARM Cortex-M Mi	crocontrollers"	', 2014, 5th						
	Edition	, Create Space Independent Publishing Platform, Un	nited States.							
5	Rulph (Chassaing and Donald Reay, Digital Signal Processi	ing and Applic	ations with the C6713						
	and C6	416 DSK, John Wiley and Sons, Inc., Publication, 2	2012 (Reprint).							
Ref	erence I	Books								
1.	Harris	and Harris, Digital Design and Computer Archite	ecture: ARM I	Edition, 2015, Morgan						
	Kaufma	ann, , United States.								
2.	Yifeng	Zhu, Embedded Systems with ARM Cortex-M Mi	crocontrollers	in Assembly Language						
	and C,	2015, 2 nd Edition, E-Man Press LLC, United States.	, , , , , ,							
3.	Avtar	Singh and S. Srinivasan, Digital Signal Process	sing – Impler	nentations using DSP						
	Microp	rocessors with Examples from TMS320C54xx, Cer	igage Learning	g India Private Limited,						
	Delhi 2									
4.	B. Ven	kataramani and M. Bhaskar, Digital Signal Process	ors – Architect	ture, Programming and						
	Applica	ations – Tata McGraw – Hill Publishing Company I	Limited. New L	Delhi, 2003.						
	ae of E	valuation: Continuous Assessment Test, Quiz, Dr	gital Assignm	ent, Final Assessment						
Tes	t.									
T	• 10	• .								
Ty	pical Pro)jects:								

- 1. Adaptive Temporal Attenuator using C5x/C6x.
- 2. Filter Design and Implementation using a Modified Prony's Method.
- 3. Voice Detection and Reverse Playback using C5x/C6x.
- 4. Acoustic Direction Tracker using C5x/C6x.
- 5. Multirate Filter using C5x/C6x.
- 6. Four-Channel Multiplexer for Fast Data Acquisition using C5x/C6x.
- 7. Video Line Rate Analysis using C5x/C6x.
- 8. Implementation of FIR High Pass Filter using ARM Cortex-M4 microcontroller.
- 9. Parametric Equalizer using STM32 microcontroller.
- 10. Noise Reduction using Moving Sum Filtering using STM32F407 Cortex M4 microcontroller.
- 11. Implementation of Audio CODEC on STM32F4 microcontroller.

12. Motor Control using PID-Controller on STM32F407 microcontroller.									
Mode of Evaluation: Project Reviews I,II,III									
Recommended by Board of Studies		12/09/2020							
Approved by Academic Council	No. 59 th	Date:	24/09/2020						

	ELECTROMAGNETIC INTERFER	ENCE					
ECE6044	AND COMPATIBILITY		L	Т	P	J	С
			3	0	0	0	3
Pre-requisite		Sylla	abus V	ersi	on :		
Course Object	lives:						
[1] Importing k	nneu al nowledge about EMI environment						
[1] Imparting K [2] Teaching Fl	MI coupling principles FMI control technique	es and desig	m of P	CBs	for I	FMC	•
[2] Feacing E	osure to EMI Standards, Regulations and Meas	surements	511 01 1	CD3	101 1		
[0] or ang only							
Expected Co	urse Outcome:						
At the end of	the course, the students will be able to						
[1]Understand t	erminologies of EMI and EMC						
[2]Analyze and	understand various EMI coupling mechanisms						
[3]List various]	EMI Test and Measurement methods						
[4] Analyze var	ious techniques needed to suppress EMI						
[5]Perceive diff	erent EMC regulations followed worldwide						
[0]ADIIIty to de	comprehend different techniques needed for Sid	anal Integri	ty and				
ability to unders	tand various models for FMI/FMC	gilai integri	ty and				
Module:1	EMI Environment	4 hours					
EMI-EMC Def	initions and units of Parameters. Sources of E	MI. conduc	cted an	d rac	liate	d EN	ΛI.
Transient EMI	,,,						,
Module:2	EMI Coupling Mechanisms	6 hours					
Conducted, F	adiated and Transient Coupling, Common	Impedance	e Grou	nd (Coup	ling	,
Radiated Con	mmon Mode and Ground Loop Coupling,	, Radiated	Diffe	renti	al N	Aode)
Coupling,		a 1	a 1.				
Near Field Ca	ble to Cable Coupling, Power Mains and Pow	er Supply	Coupli	ng.			
Module:3	ENIT Lest and Measurements	8 hours	<u>C::1:</u>		40.00	anda	
ENII Specific Military stand	and FMI Test Instruments/Systems FMI	Test EMI	Civili	an s	hon ³	arus	
Open Area To	est Site TEM Cell Antennas Conductors Se	nsors/Iniec	sinclu	ounl	ers	EMI	
Measurement		insons, mjec		oupr	C 15.		
Methods: M	ilitary Test Method and Procedures, Ca	alibration	Proce	dure	s, N	Лоde	eling
interferences.	•						U
Module:4	EMI Control Techniques	7 hours					
Shielding, Filte	ring, Grounding, Bonding, Isolation Transform	mer, Transi	ient Su	ppre	ssor	s, Ca	ble
Routing, Sign	al Control, Component Selection and M	ounting, I	Electro	statio	e di	scha	rge
protection sche	mes	-					
Module:5	EMC Standards and Regulations	5 hours		OT		<u> </u>	
CENEEC EC	Intentional standardizing organizations- FO C CE and PE standards CISPR CE and PE S	CC, CISPI Standards	K, AN IEC/EI	51, N C	DUI S etc	\mathcal{I}, Π	EC, rde
SAF Automot	ive FMC standard Frequency assignment - sn	Stanuarus,	iLC/Li iversat	ion	5 512	inua	us,
Module:6	System Design for EMC	8 hours					
PCB Traces C	Cross Talk, Impedance Control, Power I	Distribution	Dec	oupli	ng.	Zor	ning.
Motherboard De	esigns and Propagation Delay Performance N	Models. Sv	stem E	Inclo	sure	s, Po	ower
line filter placen	nent, Interconnection and Number of Printed C	Circuit Boa	rds, PC	CB a	nd su	ibsys	stem

decoupling							
Module:7	Signal Integrity and EMI/EM	AC Models	5 hours				
Effect of term	inations on line wave forms, Mat	ching scheme	es for Signal	Integrity, Effects of line			
discontinuities,	Statistical EMI/EMC models.						
Module:8	Contemporary issues:		2 hours				
	Total Lecture						
	hours:	45 hou	rs				
Text Book(s 1. Clayton Sons, No) R. Paul, Introduction to Electrom ew Jersey	agnetic com	patibility, 20	010, 2 nd ed., Wiley &			
Reference B	ooks						
 Henry W.ott, Electromagnetic Compatibility Engineering, 2011, 1sted., John Wiley and Sons, New Jersey. Patrick G. André and Kenneth Wyatt, EMI Troubleshooting Cookbook for Product Designers 2014, 1st ed., SciTech Publishing, New Jersey 							
Recommended by Board of Studies : 12/09/2020							
Approved by A	Academic Council : No: 59 th	Date :	24-09-2020				

Course Code	e Course Title		L	Т	Р	J	С				
ECE5045	ADVANCED DIGITAL IMAGE PROCESSI	CESSING 3 0 0					3				
Pre-requisite	Nil	S	Syllabus	s Ver	sion	: 1.	2				
Course Objectives:											
The course is aimed at											
[1] Revising the basics of digital image processing namely; image acquisition, digitizing, enhancing images in spatial domain, image transforms and enhancing images in frequency domain.											
[2] Enabling the students to acquire knowledge in image restoration, image compression, image segmentation and object recognition.											
[3] Motivating the students to apply image processing and classification algorithms for solving real life problems and introducing students to upcoming trends in Computer Vision.											
Course Outc	omes (CO):										
At the end of	the course the student will be able to										
[1] Comprehe	nd the image acquisition, digitization, and processing ir	spati	al doma	in.							
[2] Understan	d algorithms and programs for processing an image in t	ransfo	orm dom	ain							
[3] Acquaint	with the image enhancement and restoration techniques										
[4] Implemen	different compression techniques to compress an imag	e									
[5] Adopt diff	erent segmentation and image representation technique	s for i	mage pr	oces	sing.						
[6] Understan	d the pattern recognition approaches for implementing t	he vis	sual syst	em.							
[7] Identify co	mputer vision techniques in various real-time application	ons.									
Module:1	Image Processing in Spatial Domain7 ho	urs									
Fundamental Basic relation Transformatic Colour image	steps in DIP – Elements of visual perception - Image aship between pixels. Image enhancement - Spatia ns – Histogram Processing – Smoothing spatial filters- Processing: Models, Transformation	Samj Dor Sharp	pling an nain: B pening sj	d Qu asic patia	ianti Gre l filte	zatic y le ers.	on - evel				
Module:2	Image Transforms6 ho	urs									
<i>Image Transf</i> resolution ana and SVD	<i>forms:</i> Two dimensional Fourier Transform- Discrete lysis – Haar Transform- Discrete Wavelet Transform.	cosir Karhu	ne trans inen-Lo	form eve t	- N ranst	Iulti form	-				

Module:3	Frequency domain filtering and Image Restoration	6 hours							
Smoothing frequency domain filters- sharpening frequency domain filters- Homomorphic filtering.									
Image Restor	ation: Image deformation and geometric transform	nations, Res	storation techniques,						
Noise characterization, Linear, Position invariant degradations, Adaptive filters.									
Module:4	Image Compression	6 hours							
Image Com and MPEG	pression Techniques- Lossy and Lossless compastandards	ression- En	tropy Encoding-JPEG						
Module:5	Image Segmentation	7 hours							
Detection of segmentation	f discontinuities – point, corner, edge detection- th n-region based segmentation- morphological segn	resholding nentation - v	-edge based watershed algorithm						
Descriptors	Boundary descriptors-Region descriptors- Textur	re descriptor	rs, RANSAC.						
Module:6	RECOGNITION and CLASSIFICATION	7 hours							
structural and methods – K Region-based methods.	syntactic classifiers – Clustering techniques – sir -Means algorithm – Cluster evaluation methods. CNN, fully convolution networks, Multi-mod	nilarity mea Convolutio dal network	asures – hierarchical on neural networks, cs, Hybrid learning						
Module:7	COMPUTER VISION APPLICATIONS	4 hours							
Face recognit	ion application: personal photo collections – Insta	ince recogni	tion application :						
Location recordered regression for	ognition – Machine learning applications: Deep vo r image analysis and categorization.	ting, transfe	er learning and structured						
Module:8	Contemporary issues:	2 hours							
Total Lecture hours: 45 hrs									
Text Book(s)									
 Rafael C. Gonzalez & Richard E. Woods, "Digital Image Processing", 4th Edition, 2018, Pearson, USA David A. Forsyth and Jean Ponce, "Computer Vision: A Modern Approach", 2nd Edition, 2012, Prentice Hall, Pearson Education 									

- 1. Richard Szeliski, "Computer vision: Algorithm and Applications", Springer- Verlag, London, 2010.
- Anil K. Jain, Fundamentals of Digital Image Processing, 2015, 3rd Edition, Pearson Education, USA.
- K.P.Soman, K.I. Ramchandran, N.G.Resmi, Insights into Wavelets, From Theory to Practice, 2013, 3rd Edition, PHI Learning Private Limited, New Delhi, India.
- 4. Mark Nixon & Alberto Aguado, Feature Extraction, and Image Processing, 2013, 3rd Edition, Elsevier's Science& Technology Publications, USA

5. William K. Pratt, Digital Image Processing, 2013, John Wiley & Sons, USA.

Mode of Evaluation: Continuous Assessment Test, Quiz, Digital Assignment, Final Assessment Test.

Recommended by Board of Studies : 12/09/2020

Approved by Academic Council : 59th

Date : 24/09/2020

Course Code Course Title					P	J	С	
	FAULT TOLERANT AND DEPENDABLE							
ECE6037	CE6037 SYSTEMS					0	3	
Pre-requisite	e Nil		Syllabu	ıs Ve	rsior	1 :		
Course Object	ives:							
The course is a	med at							
[1] Providing	students with a working knowledge of the potenti	al faults a	nd errors	occu	rring			
in an embedde	d system.							
[2] Providing	knowledge in concepts of fault detection and fault	t tolerance	•					
[3] Teaching s	tudents dependability concepts							
[4] Exposing t	he fault tolerance strategies and design technique	s.						
Course Outers								
At the end of th	nes (CO):							
[1] Gain know	ledge in concepts involving fault detection							
[1] Comprehe	nd dependability concepts							
[2] Comprene	tolerance and correction mechanisms in real wo	rld scenari	05					
[4] Design and	develop dependable systems for mission critical	applicatio	ns					
[5] Understand	Fault tolerance in interconnected systems	upplicatio						
[6] Understand	Fault tolerance in distributed systems.							
[7] Apply Der	endability evaluation techniques and tools							
Module:1	Faults and Failures	4 hours						
Fault - error,	failure - faults and their manifestation - classifica	ation of fai	ilts and	failur	es			
Module:2	Dependability Concepts	5 hours						
Dependable sys	tem - techniques for achieving dependability - de	pendabilit	y measu	res				
Module:3	Fault Tolerance Strategies	6 hours	-					
Fault detection	- masking - containment - location - reconfigura	ation - reco	overy.					
Module:4	Fault tolerant design techniques	8 hours						
Hardware redu	ndancy - software redundancy - time redundancy -	- informat	ion redu	ndano	cy			
Module:5	Fault tolerance in Interconnects	6 hours						
Hypercube - sta	r graphs - fault tolerant ATM switches		-					
Module:6	Fault Tolerance in Distributed Systems	8 hours						
Byzantine General problem - consensus protocols - check pointing and recovery - stable								
storage and RAID architectures - data replication and resiliency								
Module:7 Dependability evaluation techniques and								
	tools 6 hours							
Fault trees -	Markov chains - HIMAP tool							
Module:8	Contemporary issues:	2 hours					1	
		Total Lec	ture ho	urs: 4	15 ha	ours	4	
Text Book(s)								
1. Israel Koren, C. Mani Krishna, Fault-Tolerant Systems, 2011,								

- Braci Rolen, C. Main Krisina, Fault-Tolerant Systems, 2011, Morgan Kaufmann, San Francisco.
 Elena Dubrova, Fault-Tolerant Design, 2013, Springer, Sweden.

- 1. D. P. Siewiorek and R. S. Swarz, Reliable Computer Systems: Design and Evaluation, 2014, 3rded., Digital Press, Pennsylvania.
- 2. Alessandro Birolini, Reliability Engineering: Theory and Practice, 2017, 8th ed., Springer-Verlag Berlin Heidelberg, Spain.

Mode of Evaluation: Continuous Assessment Test, Quiz, Digital Assignment, Final Assessment Test.

Recommended by Board of Studies : 12/09/2020 Approved by Academic Council : No. 59th

Date : 24/09/2020

Course Code Course Title					
ECE60	ECE6046 ADVANCED EMBEDDED PROGRAMMING				
Pre-requisite Nil					
Course Objectives:					
The course is aimed at making the students					
[1] To lear	n advanced programming skills of the Embedd	led C and Linu	ix and the		
embedded a	pplications.	ioo duimona			
[2] To deve	lop skills and understand the embedded Linux dev	ice drivers.			
<u>Expected</u> C	f the course, the student will be able to				
At the end (character driver				
[1] Develop [2] Gain kn	wiedge about advanced device driver functions				
[2] Compre	bend Linux device model				
[4] Compre	hend interrupt handlers in device drivers				
[5] Debug a	device driver code				
[6] Develor	I/O management				
[7] Develop	USB in device driver				
<u>.</u> , .,					
Module:1	Basic Device driver review	6 hours			
Boot loader	, Driver concepts -Block & character driver distin	ction -Low leve	drivers,		
etc -Writing	character drivers - Device major, minor number.		,		
Module:2	Advanced Device driver characteristics	6 hours			
Interfaces t	o driver read, write, ioctl etc-Blocking and no	n-blocking calls	s, Synchr		
Semaphores	, mutexes ,spinlocks –Proc & Sysfs interfaces	-	-		
Module:3	The Linux Device Model	6 hours			
K objects,	K sets, and Subsystems ,Low-Level Sysfs Oper	ations, Hot plug	g Event C		
Buses, Devi	ces, and Drivers, Classes, Putting It All Together,	Hot plug, Deali	ng with Fi		
Module:4	Interrupt Handling	6 hours			
Interrupts a	nd bottom halves -Writing interrupt driven dri	vers, Implemen	ting botto		
Kernel Thre	ads & Work Queues		[
Module:5	Time Delays and Debugging Techniques	6 hours	<u> </u>		
Timers, Ke	nel timers, Jiffies, Timer interrupts- Debugging	g using printing,	, querying		
and system	defaults-Debugging tools		1		
Module:6	Communicating with Hardware	6 hours			
I/O Mapped	I I/O, Memory mapped I/O, Understanding DMA	operations.			
Module:7	USB Driver Model	7 hours			
USB Devic Urbs.	e Basics, USB and Systs, USB Urbs, Writing a	USB Driver, US	B Transfe		
Iodule:8	Contemporary issues:	2 hours			
	Total Lecture hours:	45 hours			
Cext Book(s					
Cext Book (s . 1. Job) n Madieu, Linux Device Drivers Development,, 2	017, www.pack	t.com.		
Text Book(s 1. Joh Mohan La) in Madieu, Linux Device Drivers Development,, 2 I Jangir, Linux Kernel and Device Driver Program	017, www.pack ming, 2014, 1 st	t.com. Edition, U		

 Mastering Embedded Linux Programming, 2017, 2nd Edition, Packt Publishing, UK.
 Derek Molloy, Exploring Beagle Bone: Tools and Techniques for Building with Embedded Linux, 2015, 1st Edition, Wiley Publications, USA.

Mode of Evaluation: Continuous Assessment Test, Quiz, Digital Assignment, Final Assessment Test.

Recommended by Board of Studies		27/02/2016	
Approved by Academic Council	No. 40	Date	18/03/2016

Course code	Course title		L T P J C							
ECE 6047	DESIGN AND ANALYSIS OF AI	GORITHM	3 0 0 4 4							
Pre-requisite		S	Syllabus version :1							
Course Objectives:										
This course is aim	ed at									
[1] Enabling the s	tudents to carry out analysis of various alg	orithms for ma	inly time and space							
complexity.			v 1							
[2] Teaching the	[2] Teaching the students how to decide the appropriate data type and data structure for a given									
problem.		V 1	C							
[3] Teaching the	students how to select the best algorithm t	to solve a prob	olem by considering							
various problem c	haracteristics, such as the data size, the type of	of operations, e	tc.							
Expected Course	Outcome:	1								
At the end if this c	ourse, the student will be able to									
[1] Develop profic	iency in problem solving and programming.									
[2] Comprehend C	Combinatorial Optimization									
[3] Analyse variou	s algorithms for mainly time and space comp	olexity.								
[4] Comprehend C	ryptographic Algorithms	2								
[5] Learn Geomet	ric Algorithms									
[6] Analyse Parall	el Algorithms									
[7] Analyse and ev	valuate the given program in terms of code size	ze and computa	tional time.							
[8] Select the bes	t algorithm to solve a problem by consideri	ng various pro	blem characteristics,							
such as the data si	ze, the type of operations, etc.	0 1	, ,							
Module:1 Intro	duction:	7 hours								
Role of Algorith	ms in computing, Analysis of Algorithm	s, Asymptotic	notation, Euclid's							
algorithm, Proble	m, Instance, RAM model, Principles of Algo	orithm Design,	Sorting Algorithm -							
Insertion Sort &	Complexity Analysis, Divide and Conquer	Technique, So	olving recurrences -							
substitution, Iterat	ion, Recursion tree, Changing variable and M	laster's Method								
Module:2 Com	binatorial Optimization:	5 hours								
Backtracking: Dvi	namic programming: Greedy Technique : Bra	anch & Bound								
Module:3 Adva	inced Algorithmic Analysis:	5 hours								
Amortized ana	vsis: Online and offline algorith	ms: Randor	nized algorithms.							
NP Completeness										
Module:4 Crvn	tographic Algorithms:	9 hours								
Historical overvi	ew of cryptography: Private-key crypt	ography and	the key-exchange							
problem: Public-	key cryptography: Digital signatures: Secu	rity protocols:	Applications (zero-							
knowledge proofs	authentication etc.	ing protocols,	rippileations (2010							
Module:5 Geor	netric Algorithms:	7 hours								
Line segments r	properties intersections: convex hull findi	ng algorithms	Voronoi Diagram							
Delaunay Triangu	lation	ing ungoritanins,	voronor Drugrunn,							
Module:6 Para	llel Algorithms:	5 hours								
PRAM model· F	xclusive versus concurrent reads and y	vrites: Pointer	· jumping· Brent's							
theorem and work	efficiency		Jumping, Diene s							
Module:7 Distr	ibuted Algorithms:	5 hours								
Consensus and ele	ction: Termination detection: Fault tolerance	· Stabilization								
Module 8 Con	temporary issues.	2 hours								
Total Lacture has	176.		15 hours							
			45 HUUIS							

Text Book(s)

1.Anany Levitin, "Introduction to the Design and Analysis of Algorithms". 3rd edition.,2011, Addison Wesley, 2011

2. Cormen, Leiserson, Rivest and Stein, "Introduction to Algorithms", 3rd edition, McGraw-Hill, 2009

Reference Books

1. Ellis Horowitz, "Fundamentals of Computer Algorithms", 2nd Edition, Universities Press, 2008

2. M. J. Quinn, Parallel computing – theory and practice, McGraw Hill, 2002

3. Sukumar Ghosh, "Distributed Systems: An Algorithmic Approach", 1st edition, Chapman & Hall/CRC Computer & Information Science Series, 2006

4. William Stallings, "Cryptography & Network Security", 4th Edition, Prentice Hall, 2005

Mode of Evaluation: CAT / Assignment / Quiz / FAT / Project / Seminar

List of Projects (Indicative)

- I. Robot Motion Planning Based Projects to apply Computational Geometric Algorithm Principles
- II. Explore Searching Algorithms : Get into the interiors of indexing, page ranking search algorithms
- III. Design, analyze, implement and experiment new algorithms and software for solving optimization problems arising in the area of Robotics, Gaming, Telecommunication, Automotive, Genetics, Medical Applications etc.
- IV. Implement the Algorithm to cater a requirement in Military Application. The chiefcommander encrypts the command and communicates to soldiers by using DES. His command contains the data in encrypted form. Also decipher this encrypted command at the receiver.
- V. Implement the RSA Based Digital Signature scheme
- VI. Implement & Build Distributed Web Service Access (Ex : Currency Convertor)
- VII. Implement the algorithm for scheduling independent parallel tasks.
- VIII. Implement & Solve the following Algorithmic Puzzles using any Programming language
 - 1. Place N chess queens on an N×N chessboard so that no two queens attack each other using BackTracking Approach
 - 2. Implement an efficient Sudoku Solution : Given a partially filled 9×9 2D array 'grid[9][9]', the goal is to assign digits (from 1 to 9) to the empty cells so that every row, column, and subgrid of size 3×3 contains exactly one instance of the digits from 1 to 9.
 - 3. Apply Recursive principles and implement Tower of Hanoi Puzzle.

Tower of Hanoi is a mathematical puzzle where we have three rods and n disks. The objective of the puzzle is to move the entire stack to another rod, obeying the following simple rules:

1) Only one disk can be moved at a time.

2) Each move consists of taking the upper disk from one of the stacks and placing it on top of another stack i.e. a disk can only be moved if it is the uppermost disk on a stack.

3) No disk may be placed on top of a smaller disk

4. Implement an efficient program to solve the Egg Drop Puzzle involving n=2 eggs and a building with k=36 floors.

Suppose that we wish to know which stories in a 36-story building are safe to drop eggs from, and which will cause the eggs to break on landing. We make a few assumptions:

- An egg that survives a fall can be used again.
- A broken egg must be discarded.
- The effect of a fall is the same for all eggs.
- If an egg breaks when dropped, then it would break if dropped from a higher floor.
- If an egg survives a fall then it would survive a shorter fall.
- It is not ruled out that the first-floor windows break eggs, nor is it ruled out that the 36th-floor do not cause an egg to break.

If only one egg is available and we wish to be sure of obtaining the right result, the experiment can be carried out in only one way. Drop the egg from the first-floor window; if it survives, drop it from the second floor window. Continue upward until it breaks. In the worst case, this method may require 36 droppings. Suppose 2 eggs are available. What is the least number of egg-droppings that is guaranteed to work in all cases?

Implement an efficient algorithm to solve the puzzle : A man finds himself on a riverbank with a wolf, a goat, and a head of cabbage. He needs to transport all three to the other side of the river in his boat. However, the boat has room for only the man himself and one other item (either the wolf, the goat, or the cabbage). In his absence, the wolf would eat the goat, and the goat would eat the cabbage. Show how the man can get all these "passengers" to the other side

Mode of evaluation: Continuous Assessment Test, Quiz, Digital Assignment, Final Assessment Test, Project Reviews I, II, III

Recommended by Board of Studies	27/02/2016		
Approved by Academic Council	No. 40	Date	18/03/2016

Course Code	Course Title	L	Т	Р	J	С	
ECE6038	8 VIRTUAL INSTRUMENTATION SYSTEMS 0						
Pre-requisite							
Course Object	ves:						
The course is a	med at						
[1] Introducing	students on Graphical programming concepts						
[2]Exposing stu	dents to system design using block level approach						
[3]Providing ba	sic knowledge about Data Acquisition						
[4]Developing	nd solve real life problem using lab view NI based systems						
Course Outcon	nes (CO):						
At the end of th	e course the student should be able to						
[1] Acquire kn	wledge about Graphical Programming and able to differentia	te fr	om c	conv	entio	nal	
programmi	g						
[2]Learn about	basics of Graphical Programming and its structure						
[3]Understand	process of data acquisition using hardware						
[4]Provide a so	ution to engineering problem using virtual instrumentation sys	tem					
1 Lovitha Jerom	OKS e Virtual Instrumentation Using LabVIEW 2010 1st ed PHI	Lear	nina	Ind	ia		
Text Book(s)	e vintual instrumentation Using Lab view, 2010, 1st ed., 1111	Leai	ming	, mu	1a.		
1.Ian Fairw	eather, Anne Brumfield, LabVIEW: A Developer's Guide to Re	al W	/orld				
Integration,	2011, 1st ed., CRC Press, USA.						
List of Challe	nging Experiments (Indicative)						
1. Introduct	ion: Generalfunctionaldescription ofadigitalinstrum	ent-		8 h	ours		
Blockdiag	ramofaVirtual Instrument, AdvantagesofVirtualinstrum	ents					
overconve	ntionalinstruments-Architecture ofaVirtualinstrum	nent					
anditsrelat	iontotheoperatingsystem, LabVIEW – Graphicaluserinterfa	ces-					
Controlsa	dIndicators, 'G'programming – LabelsandText-Sh	ape.					
SizeandCo	lor – Ownedandfreelabels	1 /					
Lab Evor							
Examine th	e following image and develop a VI for the same						
Examine ti	e following image and develop a vi for the same						
Inp	it Array Output Array						
0	³ 0 3						
Ž.	4						
ů.	5						
Ş.	6						
24							
5 11							
8							
2. Graphica	Language: Datatype, Format, Precisionand representation	on-		8 h	ours		
Datatypes	-Dataflowprogramming, Graphical programming palettes a	nd					
tools - Fro	nt panel objects - Functions and Libraries						
anditsrelation Controlsation SizeandCo Lab Exer Examine the Image: Control state Image: Control state	Labview – Graphicaluserinteria adIndicators, 'G'programming – LabelsandText-Sha lor – Ownedandfreelabels cise: e following image and develop a VI for the same	on-		8 hc	ours		

	Lab Exercises:	
	1) Use a while loop and a waveform chart to build a VI that	
	demonstrates software timing	
	2) Develop a VI to generate a RAMP signal as shown below	
	Input to the VI are Min, Max, Time span[initial value as 0 and end value	
	only need to give] and the last input is the number of data points. VI takes	
	the difference between Max and Min and divides that interval by the number	
	of data points (# Points) that the user requires. For example this would mean	
	that the user requires 5000 points to span the difference between 0 and	
	10[time span]. In other words, the value of the ramp function at the <i>i</i> th point	
	is $((10-0)/5000)$ * <i>i</i> . The For Loop allows traversing through the values of i	
	from 0 to 5000.	
3.	Programming Structure: FORloops, WHILEloops, CASEstructure.	16 hours
5.	formulanodes Sequence structures-ArraysandClusters-Array operations-	10 110 415
	Bundle-Bundle/Unbundlebyname graphsand charts	
	Lab Exercises:	
	1) Using Error Clusters & Handling to find square root	
	2) To design an interface to measure temperature and check its range	
	between	
	• 0 to 30	
	• 30 to 60	
	• more than 60	
	Record the highest and lowest temperature. Have a switch to record the	
	selected temperature ranges.	
4.	Handling Strings: StringandfileI/O-HighlevelandLowlevelfileI/O's-	12 hours
	AttributemodesLocalandGlobal variables	
	Lab Exercises:	
	1) Design a case structured calculator using string as input cases.	
	2) Build a VI that creates an array of random numbers, scales the	
	resulting array, and takes a subset of that final array. You create a	
	For Loop that runs for 10 iterations. Eachiteration generates a	
	random number and stores it at the output tunnel. Random Array	
	displays an array of 10 random numbers. The VI multiplies each	
	value in Random Array by a Scaling Factor to create another array	
	called Final Array. The VI then takes a subset of the Final Array	
	starting at Start Subset for # of Elements and displays the subset in	
	Subset Array	
5.	Hardware Aspects: Addressingthe hardwarein LabVIEW-	8 hours
	DigitalandAnalog I/Ofunction- DataAcquisition-BufferedI/O-RealtimeData	
	Acquisition	
	Lab Exercises:	
	Build a Temperature Monitoring VI that continuously measures the	
	temperature once per time unit [variable] and displays the temperature. If the	
	temperature goes above or below the preset limits, the VI turns on a front	

	panel LED. You should be able to set the limit from the front panel. Also							
	modify the temperature monitoring VI so that it records both the highest and							
	lowest recorded temperatures, and also displays the time elapsed (in							
	seconds) since recording began. Add a save option to your temperature-							
	monitoring VI as explained above. The user will have the option to save the							
	acquired data into a spreadsheet file that will also include additional							
	information like the user name. Below shown is the Front panel for your							
	reference							
6.	Case Studies:	8 hours						
	Lab Exercises:							
	1) Interface a temperature sensor to microcontroller, acquire the sensor data and display it in labview							
	2) Interface a motor to microcontroller and control the speed of it							
	through labview.							
	Total Laboratory Hours	64 hours						
Mo	de of Evaluation:Continuous Assessment Test and Final Assessment Test							
Ty	pical Projects:							
	1. Develop a labview based system that controls the speed of a Motor. The n	notor is interfaced						
	to any Microcontroller which supports the USB communication. In Labview	w create a UI with						
	slider. The slider in the UI must be used for controlling the speed of motor.							
	2. Develop an UI in labylew that will generate a different pattern based on th	e random number						
	generated by a random function in labylew. The generated pattern must be	send out via USB						
	3 Develop on UL in Labyiew which depicts the signal generator	functionality A						
	microcontroller is interfaced with labyiew and an oscilloscope must be int	erfaced to capture						
	the signals which are given as an input in UI developed in Labyiew	enaced to cupture						
	4. Develop an UI in labyiew which acquire the sensor data and store it in an l	Excel sheet of PC.						
	The sensors are interfaced to microcontroller and the microcontroller	is interfaced to						
	labview system via USB							
Mod	de of Evaluation: Continuous Assessment Test, Final Assessment Test							
Rec	ommended by Board of Studies : 27/02/2016							

Approved by Academic Council : No:40	18/03/2016

Course cod	e	Course title	L T P J C			
ECE604	48	EMBEDDED SYSTEM DESIGN U	2 0 0 4 3			
Pre-requisi	te	Nil	yllabus version:1			
Course Ob	jectives	•				
The course i	is aime	d at				
[1] Provide	in dept	h understanding of logic and system design.				
[2] Enabling	g the stu	idents to apply their knowledge for the desig	n of advanced	digital		
hardware sy	stems v	with help of FPGA tools				
[3] Teaching	g the st	udents scheduling and communication with r	respect to FPG.	A		
Expected C	Course	Outcome:				
At the end of	of the co	ourse, the Students will be able to				
[1] Comprel	hend ov	verview of Embedded System				
[2] Learn H	ardware	e Description Languages				
[3] Acquire	abilitie	s to Design an embedded system using FPG.	A			
[4] Use Xili	nx IP C	Cores				
[5] Comprel	hend Pa	artitioning concepts				
[6] Comprel	hend So	cheduling & Communication				
[7] Identify	and exp	ploitation of Parallelism concepts				
[8] Use state	e-of-art	hardware and software to solve real life pro	blems	1		
Module:1	Emb	edded System Overview	4 hours			
H/W-FPG.	A-Emb	edded SoC and use of VLSI circuit technolog	gy-platform FF	'GA's-Altera		
Cyclone			[1		
Module:2	Hard	ware Description Languages	4 hours			
Hardware	Descrip	otion Languages - VHDL, Verilog, Other H	High-Level HD	Ls, From HDL to		
Configurat	tion Bit	-stream	r			
Module:3	Syste	em Design using FPGA	4 hours			
Principles	of syste	em design-Design quality, Modules and inter	rfaces, Abstract	tion and state,		
Cohesion a	and cou	pling, Designing and Reuse, Control flow gi	raph, Design-O	rigins of platform		
FPGA des						
Module:4	\mathbf{FPG}	A Platform	4 hours			
Componer Design Su	its, Add	ing to platform FPGA systems, assembling	custom compu	te cores. Software		
Design-Sy Root load	stem 5	onware Options, Root File system, Cross-D	evelopment 10	ois, monitors and		
Modulo:5			41			
Quartieu	Parti	titioning Problem Analytical Solution to Day	4 nours	definitions		
Overview of Partitioning Problem, Analytical Solution to Partitioning-Basic definitions, Expected performance gain, Pescurge considerations, Analytical Approach						
Module:6	Sche	duling & Communication	A hours			
Communic	ation-I	nyocation/Coordination Transfer of State P	ractical Issues-	Profiling Issues		
Data Struct	tures M	anipulate Feature Size.	100000100000	1 10111115 105000,		
Module:7	Spati	al Design	4 hours			
Principles of	of Para	llelism-Identifying Parallelism - Spatial P	arallelism wit	h Platform FPGAs-		
Parallelism	within	FPGA Hardware Cores. Parallelism within F	PGA Designs			
Module:8	Cont	emporary issues:	2hours			
		Total Lacture hours	30 hours			
		i viai Leciule nouls.	50 110015			

Text Book(s)								
1. Ron Sass, A	Andrew G Schmidt En	nbedded Systems I	Design	with Platform	n FPGAs			
Principles a	and Practices, 2011, Fi	rst Edition, Tata N	/lcGraw	/ Hill, India.				
Reference Books	5							
1. Charles H I	Roth. Jr Digital System	ns design using VI	HDL, 2	012, Re-Print	, PWS			
publishing	company (Thomson B	Books), USA.						
2. V A. Padro	ni Circuit Design with	n VHDL 2011, Firs	st Editio	on, MIT Press	5			
Cambridge	, England.	m Dagian 2011 F	lingt Edi	ition Drantia	a Hall Madam			
5. wayne wo	II, FPGA Based Syste	m Design, 2011, F	irst Ed	ition, Prentice	es Hall Modern			
Mode of Evalue	tion: Continuous Asso	account Test Ouiz	Digita	Assignmon	t Final Assassment			
Test	uon. Continuous Asse	essinent Test, Quiz	, Digite	u Assignmen	i, Filiai Assessillelli			
Typical Project	S							
1.Bluetooth based home automation using FPGA.A Bluetooth mobile app need to be developed to transfer control information to the Bluetooth receiver which is to be interfaced with the FPGA board. Based upon the received data, the household devices like lamp, fan etc. should be turned ON/OFF.								
sub divided into v register module at	various modules like v nd finally it need to be	ector address mod e integrated into a	ule, con single u	nmand regist	er module, mask plish specified tasks			
3. Implement a general purpose processor on FPGA. The purpose of the design is to build an FPGA with the following features: a CPU similar to the Atmel ATmega8, a serial port with a fixed baud rate, and an output for a single digit 7-segment display.								
4. Real-time hardware implementation of a motion detection algorithm for vision based automated surveillance systems. The working prototype of a complete standalone automated video surveillance system, including input camera interface, designed motion detection VLSI architecture, and output display interface, with real-time relevant motion detection capabilities, need to be implemented on FPGA								
Recommended by	Mode of Evaluation: Project Reviews I, II, III Recommended by Reard of Studies 27/02/2016							
Approved by Aca	demic Council	No. 40	Date	18/03/20	16			
Approved by Academic Council 100.40 Date 10/05/2010								

Course Code	Course Title			L	Т	Р	J	C
ECE5044	HARDWARE SOFTWARE CODE	3	0	0	0	3		
Pre-requisite Nil Syllabus Version: <u>1.1</u>								
Course Objective:								
The course is	aimed at		1	1		1	1	
[1] Providing	adequate knowledge in the modeling of heteroge	neous	sembedde	a syst	ems	bas	ea	on
[2] Introducir	σ the importance of estimating the cost analysis in	term	s of hardw	vare ar	nd so	oftw	are	_
parameters.	g the importance of estimating the cost unarysis in			ure ur	10 5	510.00	urv	5
[3] Introducir	g various co-synthesis and co-simulation tools for	the e	effective de	esign o	of er	nbe	dde	ed
systems with	better communication between different modules.							
Expected Co	urse Outcome:							
At the end of	the course, the Students will be able to							
[1] Apply dif	erent MOCs based on system design specification	1						
[2] Flopose a	e partitioning solution based on the algorithms	19818.						
[4] Understar	d various co-synthesis approaches.							
[5] Ability to	pre-estimate and estimate the performance metric	es for	hardware	and so	oftw	are	ba	sed
on cost analy	is.							
[6] Approxin	ate the pre-estimate and estimate the performance	ce me	etrics for s	oftwa	re t	ase	d c	ost
analysis.			- 4					
[/] Decide or	proper co-simulation method based on system spe	20111C	ation.					
Introduction	to Co-design - Comparison of co-design approache	/ -s _ I	Inified ren	resen	tati	on-I	Mo	del
– MoCs: Sta	te oriented Activity oriented Structure oriented	Data	oriented ar	nd Hei	tero	gene	201	
Software CF	SMs - Processor Characterization.	Duiu		14 110		5011		.0
Module:2	HW/SW partitioning Constraints & tradeoffs	7	hours					
Cost modelin	g, Principle of hardware/software mapping -	Rea	l time sc	hedul	ing	- (les	ign
specification	& constraints on Embedded systems - Tradeoffs							
		-	. .					
Module:3	HW/SW partitioning methodologies	7	hours	T :	41-		1	
Extended Par	Types of partitioning -Partitioning granularity	y -	Kernigan	-Lin	Alg	orit	nm	i -
Extended I di	Huoning - Dinary Farthoning, Gell Algorithm							
Module:4	Co-synthesis	7	hours					
Software sy	nthesis – Hardware Synthesis - Interface Synthesi	hesis	– Co-syn	thesis	Ap	pro	acł	nes:
Vulcan, Cosyma, Cosmos, Polis and COOL.								
Module:5	Estimation: Hardware	4	hours					
Hardware ar	ea, execution timing and power, Case studies		L					
			· · ·					
Module:6	Estimation: Software	4	hours					
Software memory and execution timing, Worst Case Execution Time, Case studies								
Module.7	Co-simulation & Co-verification	7	hours					
mouule./		1	nouis					

Principles of Co-simulation – Abstract Level; Detailed Level – Co-simulation as Partitioning	
support – Co- simulation using Ptolemy approach, Virtual Prototyping, Rapid Prototyping .	

Module:8	Contemporary issues	2	hours	
	Total Lecture:	45	hours	

Text Books:

1. Soonhoi Ha, Jürgen Teich, "Handbook of Hardware/Software Codesign", Springer , 2017.

References:

- 1. Schaumont, Patrick, A," A Practical Introduction to Hardware/Software Codesign", 2013, reprint, Springer, India.
- 2. Felice Balarin, Massimiliano Chiodo, Paolo Giusto, Harry Hsieh, Attila Jurecska, Luciano Lavagno, Claudio Passerone, Alberto Sangiovanni-Vincentelli, Ellen Sentovich, Kei Suzuki, Bassam Tabbara, "Hardware-Software Co-Design of Embedded Systems: The POLIS Approach", Springer, 2012.
- 3. http://ptolemy.eecs.berkeley.edu/ptolemyII/ptII10.0/ptII10.0.1_20141217/ptolemy/dom ains/continuous/doc/index.htm

Mode of Evaluation: CAT / Assignment / Quiz / FAT / Project / Seminar								
Recommended by Board of Studies	12/09/2020							
Approved by Academic Council	No. 59 th	Date	24/09/2020					

Course Code L T P J					С				
ECE6049MODERN AUTOMOTIVE ELECTRONICS SYSTEMS					0	4	3		
Pre-requisite Nil Syllabus Version : 1									
Course Objectives:									
The course is	The course is aimed at								
[1] Instilling	fundamental understanding of various automa	tic control s	ystems a	and b	pasic				
instrumentati	on involved in automobiles.								
[2] Learning	various automobile condition measurement and me	onitoring me	echanisr	ns.					
[3] Acqutry v	vith advanced electronic elements and their function	onal aspects	in autor	nobi	les				
Course Outc	omes (CO):								
At the end of	the course the student will be able to								
[1] Comprehe	end engine management system.								
[2] Understar	d the various Ignition and Injection systems								
[3] Explain th	e automotive control mechanisms.								
[4] Learn the	different monitoring systems for automobiles								
[5] Understar	d the typical sensors for transportation.	•							
[6] Acquire k	nowledge about upcoming trends in automotive el	ectronics sy	stems						
[7] Use the ki	nowledge attained and develop appropriate system	s for societa	al issues						
Module:1	Engine management systems	5 hours				1			
Introduction	- components for engine management system	- Open lo	op and	clos	sed 1	loop			
control syst	em – Engine cranking and warm up control –Ac	celeration, o	decelera	tion	and	1dle			
speed contro)].								
Module:2	Injection and ignition systems	5 hours							
Feedback car	buretor system–Throttle body injection and multi	point fuel in	jection s	syste	m–				
Injection syst	em controls – Advantage of electronic ignition syst	tems-Types	of solic	l stat	e igr	ntior	1		
systems and t	heir principles of operation –Electronic spark timi	ng control, l	Exhaust	emi	ssion	1			
control engin	eering	4.1							
Module:3	Automotive control mechanism	4 hours	1 1 1	•					
Electronic ma	inagement of chassis systems, Vehicle motion con	trol, anti – l	ock bral	sing	syste	em,			
Tyre pressure	monitoring system, Collision avoidance system,	Traction con	itrol syst	tem.					
Module:4	Automotive Electronics systems	4 hours	•						
Active susper	ision system Keyless entry system and Electronic	power steer	ing syste	em,					
Electronic co	ntrols - lighting design - Horn – Warning systems	s – Brake ac	tuation v	varn	ing				
systems, Info	tainment	4.1							
Module:5	Monitoring of Automotive systems	4 hours	•		•				
Speed warnin	g systems, oil pressure warning system, engine ov	er heat wari	ning sys	tem,	aır p	oress	ure		
warning syste	em, safety devices-Wind shield wiper and washer,	VANET							
Module:6	Sensors for transportation - 1	3 hours	0			,			
Basic sensor	arrangement-Types of sensors, Oxygen Sensor	r – Cranking	g Senso	r –	'OSITI	lon			
Sensors									
Module:7	Sensors for transportation - II	3 hours	1 .	•	τ7	1 • •			
Engine cool	ing water temperature Sensor–Engine oil pressure	e Sensor–Ft	iel mete	ring	-Ve	hicle	5		
speed senso	r and detonation sensor.								
Module:8	Contemporary issues:	2 hours							
Total Lecture hours: 30 hrs									
Text Book(
I. Tom D	1. Tom Denton, Automobile Electrical and Electronic Systems, 2012, 4 th Edition, Butter								
Worth	Worth Heinemann, United States								

- 2. Bosch Automotive Electrics and Automotive Electronics, 2014, 5th Edition, Springer Vieweg, United States
- Beckwith, T.G, Roy D.Marangoni, John H.Lienhard, Mechanical Measurements, 2011, 6th Edition, Addison Wesley, United States

- 1. Ernest O Doeblin, Measurement Systems, Application and design, 2013, 5th Edition McGraw Hill Book Co., United States
- 2. Holman, J.P, Experimental methods for Engineers, McGraw Hill Book Co., 2011, 8th Edition, United States
- 3. Robert Bosch Gmph, Automotive Hand Book, 2014, 9th Edition, Wiley, United States
- 4. William, B. Ribbens, Understanding Automotive Electronics, 2014, 8th Edition Butter Worth Heinemann, United States

Mode of Evaluation: Continuous Assessment Test, Quiz, Digital Assignment, Final Assessment Test.

Typical Projects

- 1. Design of Real Time Ignition Control System. Implement an automotive throttle control system using fuzzy logic approach and perform the controller synthesis in real time environment.
- 2. Develop a sliding mode controller to generate appropriate torque for the driving motor of electric vehicles that ensures optimality of the slip ratio for efficient vehicle brake.
- 3. Design a variable structure controller to deal with the strong nonlinearity of wheel slip in the design of ABS controller. Consider the several situations such as braking in dry road, wet road and snow road.
- 4. Develop a safety feature in cars to avoid colliding with a vehicle or an obstacle in the way. The main objective of the system is to help driver to prevent car collisions due to blind spots and their carelessness while driving.
- 5. Design a speed warning system (in-vehicle subsystem) that will monitor the vehicle speed and activate an auditory warning as well as record the violation when the pre-set speed limit is exceeded.

Recommended by Board of Studies : 27/02/2016		
Approved by Academic Council : No: 40	Date : 18/03/2016	

Course code Course Title L T P J C								
ECE6073		AUTOSAR AND ISO STANDARDS FOR AUTOMOTIVE SYSTEMS2002						
Pre-requisi	equisite Nil Syllabus version : 1							
Course Objectives: The course is aimed at:								
1. Enabling	the s	tudents to understand Autosar standards						
2. Introduci	ng to	the students the basic knowledge of Commu	inication Stack	t in Autosar				
3. Preparing	g the	students to understand the implementation an	nd integration	in Autosar				
Expected C	Cours	e Outcome:						
At the end of	of the	course, the student will be able to						
1.Apply the	knov	wledge of various autosar standards						
2.Analyze a	utosa	ar codes						
3.Apply the	Auto	SAR – Implementation Integration						
4.Analyze tl	he Au	utoSAR – System Services						
5. Implement	nt CA	N programming concepts through Autosar						
6. Analyze t	the IS	SO/TS 16949 standards						
7. Know the	e imp	lementation aspects of ISO/TS 16949 standa	irds					
Module:1	Aut	toSAR Standards	3 hours					
General req	uiren	nent on basic software modules - Functional	, Fault operation	on and error detection.				
Module:2	Aut	toSAR Standards – Communication	5 hours					
	Sta	ck						
Network Ma	anage	ement, TTCAN Interface standards, TTCAN	Drivers					
Module:3	Aut	toSAR – Implementation Integration	3 hours					
Platform Ty	/pes,	Memory Mapping						
Module:4	Aut	toSAR – System Services	3 hours					
Watchdog I	Mana	ger, Synchronized Time Base Manager	L					
Module:5	ISO	0/TS 16949	5 hours					
ISO/TS 169	949 -	ISO/TS 16949:2009 specifies the quality sys	stem requirem	ents for the design and				
developmen	nt, pro	oduction, installation and servicing of autom	otive related p	roducts.				
Module:6	Inti	roduction to ISO26262 Standard: Basic	3 hours					
	Cor	ncepts						
Structure of	f ISC	D26262 standard and its parts-Vocabulary	-Management	of functional Safety-				
Concept Pha	ase	1 5	U	,				
Module:7	Inti	roduction to ISO26262 Standard:	6 hours					
	Imp	plementation Aspects						
Product Dev	velop	ment System level-Product Development Ha	ardware level-I	Product Development				
Software lev	Software level-Production and Operation-Supporting Processes-ASIL Oriented and Safety							
Oriented Analysis-Guidelines on ISO26262 (Informative)-Case Studies to illustrate concepts.								
Hazard analysis and Risk assessment-Safety Goals, Preliminary Architecture-Functional Safety								
Concept								
Module:8	Cor	ntemporary Topics	2 hours					
		Total Lecture Hours:	30 hours					
Reference 1	Book	S		1				
1. Automotive Quality systems – David Hoyle, Butterworth Heinemann limited, 2000								
2. www.autosar.org								
Mode of Ev	aluat	ion: CAT / Assignment / Quiz / FAT / Project	ct / Seminar					

Mode of evaluation:							
Recommended by Board of Studies	12/09/2020						
Approved by Academic Council	No. 59	Date	24/09/2020				

ECE6092	Intelligent IoT System Design	and A	rchitect	ure	L T P J C		
Pre-	Nil				Syllabus		
requisite			Version				
	-						
Course Objec	tives:						
1. To exp	lore the characteristics of the Internet of the	ngs ai	nd its des	ign.			
2. To ena	ble the students to get familiar with lo1 arc	hitect	ure mode	IS.			
3. To acq	uaint the students with various security con	cepts	and data	analytics in tr	ie 101		
4 To day	alan and danlay an IaT anahlad prototynas	forro	al lifa na				
4. 10 dev	elop and deploy an lor enabled prototypes	101 10	ai-me us	e cases.			
Lipon complet	ion of this course, the student will be able t	0					
1 Assimi	late the technologies that enable IoT and to	inter	pret the d	ifferent comp	onents in IoT		
archite	cture.	men	prot the d				
2. Compr	ehend the concepts of edge computing a	nd ed	lge enabl	ed solutions	for real-time		
industr	ial applications.		C				
3. Envisio	on the IoT communication architecture mo	dels a	and the p	rotocol stack	for the cost-		
effectiv	e design of IoT applications on different place	latforr	ns.				
4. Interpr	et the security threats and to design a resilie	ent Io	Γ Archite	cture.			
5. Perceiv	e the data analytics tools and gain knowled	lge to	devise ar	intelligent Io	oT system.		
6. Analyz	e cloud platform services to perform IoT d	ata an	alytics an	d			
make t	he system intelligent.						
7. Design	and develop smart lo1 prototypes for use of	cases 1	under dis	cussion.			
Module:1	101 Essentials	4	nours	La for on IoT	a lution InT		
	onment Need and goals IoT Architectu	ro rof	s, Planni	adel Eurotio	solution, lo I		
IoT- Commun	ication and security Model Service oriente	ed arel	hitecture	Event-driven	architecture		
Applications a	nd standards.		intecture,		urenneeture,		
Module:2	Edge Computing	5	hours				
Introduction to	Edge/Fog computing, Edge nodes and ga	ateway	y, Node t	o edge interfa	ces, Protocol		
and standards	for edge devices, IoT edge architecture,	IoT	supported	l hardware- I	Raspberry pi,		
ARM Cortex	Processors, Software Platforms for IoT	Edge	- Raspbi	an Pi OS, R	IOT, Python		
packages for e	dge computing, Edge security, Real time ap	oplicat	tions of e	dge computin	g.		
		1	1	1	ſ		
Module:3	IoT Communication Architecture and	5	hours				
	Protocols		<u> </u>		1 1 1 1 1 1 1 1		
Communication models for IoT, 6LoWPAN, IPv4/IPv6, IoT communication protocols - MQTT,							
COAP, LOKAWAN, KILS, KPL, Communication API's.							
Madular	InT Committy and Driveou	4	hours				
INTOULIE:4	security challenges. IoT security prohitest	4 11re	A truet r	nodel Rostria	ting network		
access through security groups. Specific user access control. Data confidentiality and availability							
User Authentication/Authorization methods. Block chain for IoT security and privacy							
	success radionization methods, block cham	101 10	i securit		•		

Need for dat	a analytics, Data generation, Data pre-prod	cessin	g, Handl	ing imbalanced data sets,		
Missing valu	es, Outliers, Intelligent IoT systems –Superv	ised a	and Unsu	pervised machine learning		
algorithms, I	Deep learning for IoI- Predictive analytics,	Pythe	on functi	ons and modules for data		
analytics, Big	g Data analytics and frameworks.					
Madada	Dete Angleting in Cloud	4	1			
Module:6	Data Analytics in Cloud	4	nours	1-4		
Layered cio	for Data conter outomation Deal time alou	y in ci	loud for C	ata ala Al Samiana Data		
v intualization	no Cloud data laka Exploratory data analysi			s louis, AI Services-Data		
	ins, Cloud data lake, Exploratory data analysi	s, Op	en source	e cloud platforms and		
services.						
Modulo, 7	InT Anabitantura for apacific use apace	2	hours			
Roadman for	applete loT solution Open source loT	⊿ plotfc		Colution to Health care		
A set a set i set i set	complete for solution, Open source for		ornis, 101	d Equation to Health care,		
Automotive a	applications, Smart 101 architecture for Retain	I, LOg	gistics an	d Farming, Intelligent 101		
architecture	for Home automation, Industry applications	s, Sn	nart city	and other applications to		
cater the soci	etal requirements.					
		-	-	1		
Module:8	Contemporary Issues	2	hours			
	1		1			
	Total Lecture:	30	hours			
Text Books:						
1. Arsho	leep Bahga, Vijay Madisetti, "Internet of Thi	ngs –	A hands-	-on approach",		
Unive	ersities Press, 2015.	-				
2. John	R. Vacca, "Cloud Computing Security: Found	dation	is and Ch	allenges", CRC Press,		
2016.				-		
3. Dey, 1	Hassanien, Bhatt, Ashour and Satapathy "Inte	ernet	of Things	s and Big Data Analytics		
towar	ds Next-Generation Intelligence", Springer, 2	2018.	-			
Reference B	ooks:					
1. Adria	n McEwen & Hakim Cassimally, "Designing	the I	nternet of	f Things", Wiley, 2013.		
2. Ovidi	u Vermesan, Peter Friess, "Internet of Things	s: Cor	verging '	Technologies for Smart		
Envir	onments and Integrated Ecosystems", River I	Publis	hers, 201	3.		
3. Olivie	er Hersent, David Boswarthick, Omar Elloum	ni, "Tł	ne Interne	et of Things – Key		
applic	ations and Protocols", Wiley Publication, 20	12.				
4. Nick	Antonopoulos, Lee Gillam, "Cloud Computin	ng: Pr	inciples,	Systems and		
Appli	cations", Springer, 2010.	U	•			
5. Hwai	yu Geng, "Internet of Things and Data Analy	tics H	Iandbook	", Wiley Publishers, 2017.		
6. Rajku	mar Buyya and Satish Narayana Srirama, "F	og an	d Edge C	omputing: Principles and		
Parad	igms", Wiley series, 2019.	·	C			
Mode of Eva	luation: Continuous Assessment Test, Quiz,	Digit	tal Assign	nment and Final		
	Assessment Test.	C	U			
Typical Projects:						

4

hours

Smart Data Analytics

Module:5
- 1. Voice controlled home automation and security.
- 2. Vehicle tracking system.
- 3. Social network data analytics.
- 4. Secured edge computing with any major cloud platform.
- 5. Remote monitoring and sensing in agriculture.
- 6. Automatic parking system.
- 7. Smart retail management.
- 8. Predictive analytics in health care.
- 9. Warehousing and logistics system.
- 10. Water flow monitoring and management.

Mode of Evaluation: Project Reviews I,II and III							
Recommended by Board of Studies		12/09/2020					
Approved by Academic Council	No. 59 th	Date	24/09/2020				

Course Cod	e Course Title		L	Т	Р	J	С		
ECE 6093	Advanced Machine Leaning and Deep I	Learning	3	0	0	0	3		
Pre-requisit	e Nil	S	yllabus	Ver	sion	: 1.	0		
Course Objectives:									
The course is aimed at									
[1] Understanding about the fundamentals of machine learning and neural networks									
[2] Enabling	he students to acquire knowledge about pattern re	cognition.							
[3] Motivatin	g the students to apply deep learning algorithms for	or solving re	al life p	roble	ems.				
Course Outc	omes (CO):								
At the end of	the course the student will be able to								
[1] Comprehe	[1] Comprehend the categorization of machine learning algorithms.								
[2] Understan	d the types of neural network architectures, activa	tion functio	ns						
[3] Acquaint	with the pattern association using neural networks								
[4] Explore v	arious terminologies related with pattern recognition	on							
[5] Adopt different feature selection and classification techniques									
[6] Understand the architectures of convolutional neural networks									
[7] Comprehend advanced neural network architectures such as RNN, Autoencoders, and GANs.									
Module:1	Learning Problems and Algorithms	4 hours							
Various paradigms of learning problems, Supervised, Semi-supervised and Unsupervised algorithms									
Module:2	Neural Network – I	6 hours							
Differences between Biological and Artificial Neural Networks - Typical Architecture, Common Activation Functions, Multi-layer neural network, Linear Separability, Hebb Net, Perceptron, Adaline, Standard Back propagation									
Module:3	Neural Network – II	6 hours							
Training Algo	prithms for Pattern Association - Hebb rule and De	elta rule, He	tero asso	ociat	ive,	Auto)		
associative, Kohonen Self Organising Maps, Examples of Feature Maps, Learning Vector									
Quantization,	Gradient descent, Boltzmann Machine Learning								

Module:4	Μ	achine Learning: Terminologies	7 hours		
Classifying	San	pples: The confusion matrix, Accuracy, Precis	sion, Recall	, F1- Score, the curse	
of dimensionality, training, testing, validation, cross validation, overfitting, under-fitting the					
data, early s	stopp	bing, regularization, bias and variance			
Module:5	M	achine Learning: Feature Selection and			
	C	assification	6 hours		
Feature Sele trees, Naïve	ectic e Bay	on, normalization, dimensionality reduction, C yes, Binary classification, multi class classification	Classifiers: 1 ation, cluste	KNN, SVM, Decision ring.	
Module:6	C	onvolutional Neural Networks	7 hours		
Feed forward	d ne	tworks, Activation functions, backpropagation	on in CNN	, optimizers, batch	
normalization of CNNs.	n, co	nvolution layers, pooling layers, fully connection	cted layers,	dropout, Examples	
Module:7	R	NNs, Autoencoders and GANs	7 hours		
State, Structu	ire o	f RNN Cell, LSTM and GRU, Time distribute	d layers, Ge	enerating Text,	
Autoencoders	s: Co	onvolutional Autoencoders, Denoising autoenco	coders, Vari	ational autoencoders,	
GANs: The d	liscri	minator, generator, DCGANs			
Module:8	0	Contemporary issues:	2 hours		
			Tota	ll Lecture hours: 45 hrs	
Text Book((s)				
2 1 5 0	Ion	C T Sun E Migutoni Nouro Euggu and	l Soft Com	auting A	
5. J. S. K. Jang, C. I. Sun, E. Mizutani, Neuro Fuzzy and Soft Computing - A Computational Approach to Learning and Machine Intelligence 2012, PHI					
learning					
4. Deep Learning, Ian Good fellow, Yoshua Bengio and Aaron Courville, MIT Press, ISBN:					
9780262035613, 2016.					
Reference l	Bool	ΣS			
6. The E	leme	ents of Statistical Learning. Trevor Hastie, Rol	bert Tibshir	ani and Jerome	
Friedi 7 Patter	man. n Re	Second Edition. 2009.	Bishon Sn	ringer 2006	
8. Understanding Machine Learning. Shai Shalev-Shwartz and Shai Ben-David. Cambridge					
Unive	ersity	Press. 2017.			
Assessment	t Tes	ation: Continuous Assessment Test, Quiz, Dig t.	gital Assign	ment, Final	
Recommend	ded l	by Board of Studies : 12/09/2020			
Approved by	Aca	idemic Council : 59 th	Dat	e : 24/09/2020	
Course code	;	Scripting Languages For Design	Automatio	n LTPJC	

ECE 6094			2 0 2 0 3
Pre-requisite	ECE5043 Embedded Programming		Syllabus version
			v. 1.0
Course Obje	ctives :		
The course is	aimed to motivate the students to		
1. Work	in LINUX environment.		
2. Devel	op the PERL scripts		
3. Devel	op the TCL & TK scripts for automation		
4. Devel	op the python scripts for automation		
Expected Co	una Outcomo e		
Expected CO	the course the students will be able to		
At the end of 1	rehand PEPI . Concerns and its range of application	a to which the	y or a guitad
1. Comp	on skills and understanding DERI	is to which the	y are surred
2. Devel 3. Under	estanding the basics of TCL scripts		
4 Comr	rehend the concept of Tk		
5 Get ir	troduced to Python Programming		
6 Devel	on programming skills on python functions		
7. Under	standing the OOP and exception Handling using p	vthon	
8. Exper	tise in Scripting language	,	
Module:1	PERL	4 hours	
History and (Concepts of PERL - Scalar Data - Arrays and List	Data - Control	structures – Hashes -
Basics I/O - I	Regular Expressions – Functions - Miscellaneous co	ontrol structure	s - Formats.
Module:2	Advanced Topics in PERL	4 hours	
Directory acc	ess - File and Directory manipulation - Process Ma	nagement - Pac	ckages and Modules.
		1	
Module:3	<u>rcl</u>	4 hours	
An Overview	of TCL and TK -TCL Language syntax - Varial	bles – Expressi	ions – Lists - Control
flow – procee	ures - Errors and exceptions - String manipulations	8.	
			1
Module:4	Advanced Topics in TCL	4 hours	
Accessing fil	es- Processes. Applications - Controlling Tools - Ba	asics of TK.	
Module:5	Python	4 hours	
Introduction	to Python, Objects: strings, lists, dictionary, tuple,	files, Looping	constructs
Madulad	Dethans Frenchions and Madulas	1 h anna	
Eurotional h	rython: Functions and Modules nockages (interm	+ nours	decomptons
Functions: C	asies, scope, arguments, Modules: packages (mem	and external), decorators
Modulo.7	Duthan, OOD and Examplian Uandling	1 hours	
OOP: class	y operator overloading designing with classe	+ nours	avantion objects
designing w	th exceptions. Meta classes	s, Exceptions.	exception objects,
	ווו כתכברווסווס, ויוכומ-כומסספס		
Module 8	Contemporary issues:	2 hours	
1000010.0	Company address		
	Fotal Lecture hours:	30 hours	
	- viui 2/viui v 11vul 9i		

Ref	erence Books						
1.	Guido van Rossum Fred L. Drake, Jr., editor, "Python Tutorial Release 3.2.3", 2012	2.					
2.	Larry Wall, Tom Christiansen, John Orwant, "Programming PERL", Oreilly Publications, Fourth Edition, 2012.						
3.	John K. Ousterhout, Ken Jones, "TCL and the TK Toolkit", Pearson Education, Second Edition, 2010.						
4.	Eric Matthes, "Python Crash Course: A Hands-on, Project-based Introduction to Programming",						
	Second Edition, No starch press, 2019						
Мо	de of Evaluation: CAT / Assignment / Quiz / FAT / Project / Seminar						
List	t of Challenging Experiments (Indicative)						
1.	PERL:	8 hours					
	• Write a script that computes the average of each column in a table of data						
	• Write a script extracts a subset of docs from a database						
	• Write a script does "string replacement" on the standard input						
2.	TCL/TK:	8 hours					
	• Develop a clock that shows time either analog or digital						
	• Develop a small calculator in Tcl/Tk. In addition to the buttons on screen, use any of expr's other functionalities via keyboard input.						
	• Write a script that allows doodling (drawing with the mouse)						
3.	Python:	8 hours					
	• Python Implementation of Mutual-Exclusion (MUTEX algorithm) for						
	Embedded operating systems						
	Python Implementation of Round Robin Scheduling for Embedded OS						
4.	Verification automation tool development using Perl/Python scripts	6 hours					
Tot	al Laboratory Hours	30 hours					
Mo	de of evaluation: Continuous Lab Assessment						
Rec	commended by Board of Studies 12/09/2020						
App	proved by Academic Council No. 59 th Date 24/09/2020						

Course Code	Course Title			Т	Р	J	С
CSE6052	PARALLEL PROCESSING AND COMPUTING			0	0	0	3
Pre-requisite	Nil	Syllabus Version : 1					
Course Objectives:							

The course is aimed at [1] Teaching the students to understand the scope, design and model of parallelism and to know the parallel computing architecture [2]Teaching students to do analytical modelling and performance of parallel programs [3]Teaching students to solve a complex problem with message passing model [4] Programming with CUDA and analyse complex problems with shared memory programming **Course Outcomes (CO):** At the end of the course the student will be able to [1] Understand the fundamentals of parallel processing [2] Illustrate the scheduling loops and process execution [3] Realize the parallel system architecture with CUDA [4] Comprehend the kernel based parallel programming concepts [5] Apply the performance consideration for parallel processing [6] Analyse various parallel computation patterns [7] Perform spare matrix vector multiplications **Introduction to Parallel Processing** Module:1 5 hours Parallel processing - Concepts and Terminology- Parallel Computer Memory Architectures -Parallel Programming Models - Designing Parallel Programs- Performance Analysis Module:2 **Shared Memory Programming** 6 hours Processes and Threads - Scope of Variables - Reduction Clause - Directives - Scheduling Loops -Caches, Cache coherence and False Sharing - Thread Safety - Examples: Bubble-sort, Odd- even transposition sort Module:3 **Parallel Computing** 6 hours Portability and Scalability- Introduction to CUDA, Data Parallelism and Threads-Memory Allocation and Data Movement API- Kernel-Based SPMD Parallel Programming-Kernel based Parallel Programming, Multidimensional Kernel Configuration- Basic Matrix-Matrix Multiplication **Kernel-Based Parallel Programming** Module:4 6 hours Thread Scheduling-Control Divergence- Memory Model and Locality - CUDA Memories-Tiled Parallel Algorithms- Tiled Matrix Multiplication- Tiled Matrix Multiplication Kernel-Handling Boundary Conditions in Tiling-- A Tiled Kernel for Arbitrary Matrix Dimensions **Performance Considerations** Module:5 6 hours Warps and Thread execution - Global Memory Bandwidth - DRAM Bandwidth -Memory Coalescing -Dynamic partition of execution resources **Parallel Computation Patterns** Module:6 8 hours Convolution- Tiled Convolution- 2D Tiled Convolution Kernel- Data Reuse in Tiled Convolution-Reduction- A Basic Reduction Kernel- Scan (Prefix Sum) - A Work-Inefficient Scan Kernel- A Work-Efficient Parallel Scan Kernel Sparse Matrix Vector Multiplication Module:7 6 hours Parallel SpMV Using CSR-Padding and Transposition-Using Hybrid to Control Padding-Sorting and Partitioning for Regularization Module:8 **Contemporary issues:** 2 hours **Total Lecture hours: 45 hrs Text Book(s)** 1. Ananta Grama, Anshul Gupta, George Karypis, Vipin Kumar, Introduction to Parallel Computing, 2011, Second Edition, Addison Wesley Professional, UK. 2. David B. Kirk and Wen-mei W. Hwu, Programming Massively Parallel Processors: A Hands-on Approach, 2016, Third Edition, Morgan Kaufmann Publishers, US.

Reference Books

1. Pacheco, Peter. An Introduction to Parallel programming, 2011, First Edition, Morgan Kaufmann Publishers, USA

Mode of Evaluation: Continuous Assessment Test, Quiz, Digital Assignment, Final Assessment Test.

Recommended by Board of Studies : 27/02/2016

Approved by Academic Council : No. 40 Date : 18/03/2016