

### **School of Electronics Engineering**

M. Tech. – Embedded Systems

Curriculum and Syllabus

(2024-25 Admitted Students)

### VISION STATEMENT OF VELLORE INSTITUTE OF TECHNOLOGY

Transforming life through excellence in education and research.

### MISSION STATEMENT OF VELLORE INSTITUTE OFTECHNOLOGY

World class Education: Excellence in education, grounded in ethics and critical thinking, for improvement of life.

**Cutting edge Research**: An innovation ecosystem to extend knowledge and solve critical problems.

Impactful People: Happy, accountable, caring and effective workforce and students.

Rewarding Co-creations: Active collaboration with national & international industries & universities for productivity and economic development.

Service to Society: Service to the region and world through knowledge and compassion.

### VISION STATEMENT OF THE SCHOOL OF ELECTRONICS ENGINEERING

To be a leader by imparting in-depth knowledge in Electronics Engineering, nurturing engineers, technologists and researchers of highest competence, who would engage in sustainable development to cater the global needs of industry and society.

### MISSION STATEMENT OF THE SCHOOL OF ELECTRONICS ENGINEERING

- Create and maintain an environment to excel in teaching, learning and applied research in the fields of electronics, communication engineering and allied disciplines which pioneer for sustainable growth.
- Equip our students with necessary knowledge and skills which enable themto be lifelong learners to solve practical problems and to improve the quality of human life

### PROGRAMME EDUCATIONAL OBJECTIVES (PEOs)

### The graduates of the programme will be able to

- 1. Graduates will be engineering practitioners and leaders, who would help solve industry's technological problems
- 2. Graduates will be engineering professionals, innovators or entrepreneurs engaged in technology development, technology deployment, or engineering system implementation in industry
- 3. Graduates will function in their profession with social awareness and responsibility
- 4. Graduates will interact with their peers in other disciplines in industry and society and contribute to the economic growth of the country
- 5. Graduates will be successful in pursuing higher studies in engineering or management
- 6. Graduates will pursue career paths in teaching or research

.

### **PROGRAMME OUTCOMES (POs)**

On completion of the Programme the students will have the

- PO\_01: Having an ability to apply mathematics and science in engineering applications.
- PO\_02: Having an ability to design a component or a product applying all the relevant standards and with realistic constraints, including public health, safety, culture, society and environment
- PO\_03: Having an ability to design and conduct experiments, as well as to analyse and interpret data, and synthesis of information
- PO\_04: Having an ability to use techniques, skills, resources and modern engineering and IT tools necessary for engineering practice
- PO\_05: Having problem solving ability- to assess social issues (societal, health, safety, legal and cultural) and engineering problems
- PO\_06: Having adaptive thinking and adaptability in relation to environmental context and sustainable development
- PO\_07: Having a clear understanding of professional and ethical responsibility
- PO\_08: Having a good cognitive load management skills related to project management and finance

### **Programme Specific Outcomes (PSOs)**

On completion of M. Tech. Embedded Systems, graduates will be able to

PSO1. Apply the advanced concepts of Embedded System Design with realtime constraints using advanced Microcontrollers and FPGA based systems.

PSO2. Use the cutting-edge technologies in both hardware and software, to solve real- world multi-disciplinary problems and arrive at a viable solution.

PSO3. Independently carry out research on diverse Embedded System strategies to address practical problems and present a substantial technical report.

	CREDIT INFO							
S.no	Catagory	Credits						
1	Discipline Core	24						
2	Discipline Elective	12						
3	Projects and Internship	26						
4	Open Elective	3						
5	Skill Enhancement	5						
	Total Credits 70							

	Discipline Core								
sl.no	Course Code	Course Title	Course Type	Ver sio n	L	Т	Р	J	Credits
1	MEDS501L	Embedded System Design	Theory Only	1.0	3	0	0	0	3.0
2	MEDS502L	Microcontroller Architecture and Organization	Theory Only	1.0	3	0	0	0	3.0
3	MEDS502P	Microcontroller Architecture and Organization Lab	Lab Only	1.0	0	0	2	0	1.0
4	MEDS503L	Embedded Programming	Theory Only	1.0	3	0	0	0	3.0
5	MEDS503P	Embedded Programming Lab	Lab Only	1.0	0	0	2	0	1.0
6	MEDS504L	In Vehicle Networking	Theory Only	1.0	3	0	0	0	3.0
7	MEDS505L	Real Time Operating System	Theory Only	1.0	3	0	0	0	3.0
8	MEDS505P	Real Time Operating System Lab	Lab Only	1.0	0	0	2	0	1.0
9	MEDS506L	Wireless and Mobile Communication	Theory Only	1.0	3	0	0	0	3.0
10	MEDS507L	Electronic Hardware System Design	Theory Only	1.0	2	0	0	0	2.0
11	MEDS507P	Electronic Hardware System Design Lab	Lab Only	1.0	0	0	2	0	1.0

	Discipline Elective								
sl.no	Course Code	Course Title	Course Type	Ver sio n	L	Т	Р	J	Credits
1	MEDS601L	Electromagnetic Interference and Compatibility	Theory Only	2.0	3	0	0	0	3.0
2	MEDS602L	Advanced Digital Image Processing	Theory Only	1.0	3	0	0	0	3.0
3	MEDS603L	Design and Analysis of Algorithms	Theory Only	1.0	3	0	0	0	3.0
4	MEDS605L	Hardware Software Co-design	Theory Only	1.0	2	0	0	0	2.0
5	MEDS606L	Modern Automotive Electronics Systems	Theory Only	1.0	3	0	0	0	3.0
6	MEDS608L	Intelligent IoT System Design and Architecture	Theory Only	1.0	2	0	0	0	2.0
7	MEDS608P	Intelligent IoT System Design and Architecture Lab	Lab Only	1.0	0	0	2	0	1.0
8	MEDS609L	Fault Tolerance and Dependable Systems	Theory Only	1.0	3	0	0	0	3.0
9	MEDS611L	Parallel Processing and Computing	Theory Only	1.0	3	0	0	0	3.0
10	MEDS613L	Cloud computing	Theory Only	1.0	3	0	0	0	3.0
11	MEDS614L	Cyber Physical Systems	Theory Only	1.0	3	0	0	0	3.0
12	MEDS614P	Cyber Physical Systems Lab	Lab Only	1.0	0	0	2	0	1.0
13	MEDS615L	5G and Future Generation Communication Systems	Theory Only	1.0	3	0	0	0	3.0
14	MEDS616L	Machine Learning and Deep Learning	Theory Only	1.0	3	0	0	0	3.0

Report On: 13-02-2024 03:47:23 PM Page 1 of 3

	Discipline Elective								
15	MVLD611L	Advanced Computer Architecture	Theory Only	1.0	3	0	0	0	3.0
16	MVLD613L	System Design with FPGA	Theory Only	1.0	3	0	0	0	3.0
17	MVLD616L	Scripting Language for Electronic Design Automation	Theory Only	1.0	3	0	0	0	3.0

	Projects and Internship								
sl.no	Course Code	Course Title	Course Type	Ver sio	L	Т	Р	J	Credits
				n					
1	MEDS696J	Study Oriented Project	Project	1.0	0	0	0	0	2.0
2	MEDS697J	Design Project	Project	1.0	0	0	0	0	2.0
3	MEDS698J	Internship I/ Dissertation I	Project	1.0	0	0		0	10.0
4	MEDS699J	Internship II/ Dissertation II	Project	1.0	0	0	0	0	12.0

	Open Elective								
sl.no	Course Code	Course Title	Course Type	Ver sio n	L	т	Р	J	Credits
1	MFRE501L	Francais Fonctionnel	Theory Only	1.0	3	0	0	0	3.0
2	MGER501L	Deutsch fuer Anfaenger	Theory Only	1.0	3	0	0	0	3.0
3	MSTS601L	Advanced Competitive Coding	Soft Skill	1.0	3	0	0	0	3.0

	Skill Enhancement								
sl.no	Course Code	Course Title	Course Type	Ver sio n	L	т	Р	J	Credits
1	MENG501P	Technical Report Writing	Lab Only	1.0	0	0	4	0	2.0
2	MSTS501P	Qualitative Skills Practice	Soft Skill	1.0	0	0	3	0	1.5
3	MSTS502P	Quantitative Skills Practice	Soft Skill	1.0	0	0	3	0	1.5

**Report On: 13-02-2024 03:47:23 PM** Page 2 of 3

Course Code	Course Title	L	Т	Р	С
MEDS501L Embedded System Design		3	0	0	3
Pre-requisite	NIL S	yllab	us v	ers	ion
		1.0			
0 1 1					

The course aimed at

- 1. Ability to understand comprehensively the technologies and techniques underlying in building an embedded solution to a wearable, mobile and portable system.
- 2. Analyze UML diagrams and advanced Modelling schemes for different use cases.
- 3. Understand the building process of embedded systems

### **Course Outcome**

The students will be able to

- 1. Define an embedded system and compare with general purpose system.
- 2. Appreciate the methods adapted for the development of a typical embedded system.
- 3. Get introduced to RTOS and related mechanisms.
- 4. Classify types of processors and memory architecture
- 5. Differentiate the features of components and networks in embedded systems
- 6. Develop real-time working prototypes of different small-scale and medium-scale embedded Systems.
- 7. Apprehend the various concepts in Multi-Tasking

### Module:1 Introduction to Embedded System 5 hours Embedded system processor, hardware unit, software embedded into a system, Example of an embedded system, Embedded Design life cycle, Layers of Embedded Systems. Module:2 | Embedded System Design Methodologies Embedded System modelling [FSM, SysML, MARTE], UML as Design tool, UML notation, Requirement Analysis and Use case Modelling, Design Examples Module:3 Building Process For Embedded Systems 4 hours Preprocessing, Compiling, Cross Compiling, Linking, Locating, Compiler Driver, Linker Map Files, Linker Scripts and scatter loading, Loading on the target, Embedded File System. Module:4 | System design using general purpose 7 hours processor Microcontroller architectures (RISC, CISC), Embedded Memory, Strategic selection of processor and memory, Memory Devices and their Characteristics, Cache Memory and Various mapping techniques, DMA. Module:5 Component Interfacing & Networks 9 hours Memory Interfacing, I/O Device Interfacing, Interrupt Controllers, Networks for Embedded systems- USB, PCI,PCI Express, UART, SPI, I2C, CAN, Wireless Applications - Bluetooth, Zigbee, Wi-Fi., 6LoWPAN, Evolution of Internet of things (IoT). Module:6 Operating Systems 7 hours Introduction to Operating Systems, Basic Features & Functions of an Operating System, Kernel & its Features [polled loop system, interrupt driven system, multi rate system], Processes/Task and its states, Process/Task Control Block, Threads, Scheduler, Dispatcher. Module:7 | Multi Tasking 6 hours Context Switching, Scheduling and various Scheduling algorithms, Inter-process Communication (Shared Memory, Mail Box, Message Queue), Inter Task Synchronization (Semaphore, Mutex), Dead Lock, Priority Inversion (bounded and unbounded), Priority Ceiling Protocol & Priority Inheritance Protocol Module:8 Contemporary Issues 2 hours **Total Lecture hours:** 45 hours

# Text Book(s) Raj Kamal, "Embedded systems Architecture, Programming and Design", Tata McGraw- Hill, 2016. Wayne Wolf "Computers as components: Principles of Embedded Computing System Design", The Morgan Kaufmann Series in Computer Architecture and Design, 2013. Reference Books Lyla B. Das," Embedded Systems an Integrated Approach", Pearson Education, 2013. Shibu K V," Introduction to Embedded Systems", McGraw Hill Education(India) Private Limited, 2014 Sriram V Iyer, Pankaj Gupta " Embedded Real Time Systems Programming", Tata McGraw- Hill, 2012

4.	Steve Heath, "Embedded Systems	Design", EDN Series, 2013.					
Мо	Mode of Evaluation: Continuous Assessment, Digital Assignment, Quiz and Final						
Ass	sessment Test						
Г.	a compared at level De and of Ctualine	00.07.0000					

Recommended by Board of Studies	28-07-2022		
Approved by Academic Council	No. 67	Date	08-08-2022

Course Code			L	Т	Р	С
MEDS502L Microcontroller Architecture and Organization			3	0	0	3
Pre-requisite	te NIL Syllabus v		ers	ion		
		1.0				

The course aimed at

- 1. Describing the architecture of 8051 microcontroller and ARM processor
- 2. Teaching the instruction set of 8051 and ARM microcontroller to efficient programs
- 3. Designing system in block level using microcontroller, memory devices, buses and other peripheral devices
- 4. Solving real life problem using microcontroller-based systems

### Course Outcome

At the end of the course, the students will be able to

1. Describe the architectures of processors

Edition, Elsevier, United States

- 2. Develop Assembly program applying Digital logic and mathematics using 8051
- 3. Develop Assembly Language Program for ARM
- 4. Develop ALP with minimum instructions and memory.
- 5. Analyze and evaluate the given program in terms of code size and computational time
- 6. Design Microcontroller based system within realistic constraint like user specification, availability of components etc
- 7. Solve real life problem and construct a complete system as a solution

Module:1Introduction to Microcontrollers5 hoursMicroprocessors Vs Microcontrollers; Classification – bits, memory architecture, ISA; LittleEndian Vs Big Endian.6 hoursArchitecture – Timers, Interrupts, Register Architecture (banks), PSW register, Memory architecture; Instruction set.8 hoursModule:38051 Programming and Interfaces8 hoursProgramming in C & Assembly for – Interrupts, Timers and Interfaces – PORTS, LED, ADC, SENSORS, LCD, DAC, Serial Communication4 hoursModule:4ARM Architecture4 hoursARM Design Philosophy; Overview of ARM architecture; States [ARM, Thumb, Jazelle]; Registers, Modes; Conditional Execution; Pipelining; Vector Tables; Exception handling.Module:5ARM Instruction- data processing instructions, branch instructions, load store instructions, SWI instruction, Loading instructions, conditional Execution, Assembly Programming.Module:6Thumb Instruction Set6 hoursThumb Instruction-Thumb Registers, ARM Thumb interworking, branch instruction, data processing instruction, single/multiple load store instruction, Stack instruction, SWI instruction, Assembly Programming.8 hoursModule:7ARM Core based Microcontroller8 hoursArchitecture of LPC214X, Memory Addressing, IO ports, Timers/counter, Watch Dog Timer, PWM, ADC/DAC, UART, Interrupts, Displays, C programming.Module:8Contemporary Issues2 hours									
Module:2   8051 Microcontroller   6 hours	Module:1	Introduction to Microcontrollers	5 hours						
Architecture - Timers, Interrupts, Register Architecture (banks), PSW register, Memory architecture; Instruction set.    Module:3   8051 Programming and Interfaces   8 hours	Microproce	essors Vs Microcontrollers; Classification - bits,	memory architecture, ISA; Little						
Architecture - Timers, Interrupts, Register Architecture (banks), PSW register, Memory architecture; Instruction set.  Module:3 8051 Programming and Interfaces 8 hours  Programming in C & Assembly for - Interrupts, Timers and Interfaces - PORTS, LED, ADC, SENSORS, LCD, DAC, Serial Communication  Module:4 ARM Architecture 4 hours  ARM Design Philosophy; Overview of ARM architecture; States [ARM, Thumb, Jazelle]; Registers, Modes; Conditional Execution; Pipelining; Vector Tables; Exception handling.  Module:5 ARM Instruction Set 6 hours  ARM Instruction- data processing instructions, branch instructions, load store instructions, SWI instruction, Loading instructions, conditional Execution, Assembly Programming.  Module:6 Thumb Instruction Set 6 hours  Thumb Instruction-Thumb Registers, ARM Thumb interworking, branch instruction, data processing instruction, single/multiple load store instruction, Stack instruction, SWI instruction, Assembly Programming.  Module:7 ARM Core based Microcontroller 8 hours  Architecture of LPC214X, Memory Addressing, IO ports, Timers/counter, Watch Dog Timer, PWM, ADC/DAC, UART, Interrupts, Displays, C programming.									
ARM Instruction data processing instructions, conditional Execution, Loading instruction, Loading instructions, SWI instruction, Thumb Instruction Set  Thumb Instruction, Assembly Programming.  Module:7   ARM Core based Microcontroller Module:7   ARM Core Construction Set  ARM Design Philosophy; Overview of ARM architecture; States [ARM, Thumb, Jazelle]; Registers, Modes; Conditional Execution; Pipelining; Vector Tables; Exception handling.  Module:5   ARM Instruction Set   Ghours    6 hours   ARM Instruction-data processing instructions, branch instructions, load store instructions, SWI instruction, Loading instructions, conditional Execution, Assembly Programming.  Module:6   Thumb Instruction Set   Ghours    Thumb Instruction-Thumb Registers, ARM Thumb interworking, branch instruction, data processing instruction, single/multiple load store instruction, Stack instruction, SWI instruction, Assembly Programming.  Module:7   ARM Core based Microcontroller   8 hours    Architecture of LPC214X, Memory Addressing, IO ports, Timers/counter, Watch Dog Timer, PWM, ADC/DAC, UART, Interrupts, Displays, C programming.	Module:2	8051 Microcontroller	6 hours						
architecture: Instruction set.Module:38051 Programming and Interfaces8 hoursProgramming in C & Assembly for – Interrupts, Timers and Interfaces – PORTS, LED, ADC, SENSORS, LCD, DAC, Serial CommunicationModule:4ARM Architecture4 hoursARM Design Philosophy; Overview of ARM architecture; States [ARM, Thumb, Jazelle]; Registers, Modes; Conditional Execution; Pipelining; Vector Tables; Exception handling.Module:5ARM Instruction Set6 hoursARM Instruction- data processing instructions, branch instructions, load store instructions, SWI instruction, Loading instructions, conditional Execution, Assembly Programming.Module:6Thumb Instruction Set6 hoursThumb Instruction-Thumb Registers, ARM Thumb interworking, branch instruction, data processing instruction, single/multiple load store instruction, Stack instruction, SWI instruction, Assembly Programming.Module:7ARM Core based Microcontroller8 hoursArchitecture of LPC214X, Memory Addressing, IO ports, Timers/counter, Watch Dog Timer, PWM, ADC/DAC, UART, Interrupts, Displays, C programming.	Architectur	re - Timers, Interrupts, Register Architecture	(banks), PSW register, Memory						
Programming in C & Assembly for – Interrupts, Timers and Interfaces – PORTS, LED, ADC, SENSORS, LCD, DAC, Serial Communication  Module:4   ARM Architecture   4 hours    ARM Design Philosophy; Overview of ARM architecture; States [ARM, Thumb, Jazelle]; Registers, Modes; Conditional Execution; Pipelining; Vector Tables; Exception handling.  Module:5   ARM Instruction Set   6 hours    ARM Instruction- data processing instructions, branch instructions, load store instructions, SWI instruction, Loading instructions, conditional Execution, Assembly Programming.  Module:6   Thumb Instruction Set   6 hours    Thumb Instruction-Thumb Registers, ARM Thumb interworking, branch instruction, data processing instruction, single/multiple load store instruction, Stack instruction, SWI instruction, Assembly Programming.  Module:7   ARM Core based Microcontroller   8 hours    Architecture of LPC214X, Memory Addressing, IO ports, Timers/counter, Watch Dog Timer, PWM, ADC/DAC, UART, Interrupts, Displays, C programming.	architecture	e; Instruction set.							
Module:4 ARM Architecture 4 hours  ARM Design Philosophy; Overview of ARM architecture; States [ARM, Thumb, Jazelle]; Registers, Modes; Conditional Execution; Pipelining; Vector Tables; Exception handling.  Module:5 ARM Instruction Set 6 hours  ARM Instruction- data processing instructions, branch instructions, load store instructions, SWI instruction, Loading instructions, conditional Execution, Assembly Programming.  Module:6 Thumb Instruction Set 6 hours  Thumb Instruction-Thumb Registers, ARM Thumb interworking, branch instruction, data processing instruction, single/multiple load store instruction, Stack instruction, SWI instruction, Assembly Programming.  Module:7 ARM Core based Microcontroller 8 hours  Architecture of LPC214X, Memory Addressing, IO ports, Timers/counter, Watch Dog Timer, PWM, ADC/DAC, UART, Interrupts, Displays, C programming.	Module:3	8051 Programming and Interfaces	8 hours						
ARM Design Philosophy; Overview of ARM architecture; States [ARM, Thumb, Jazelle]; Registers, Modes; Conditional Execution; Pipelining; Vector Tables; Exception handling.  Module:5 ARM Instruction Set 6 hours  ARM Instruction- data processing instructions, branch instructions, load store instructions, SWI instruction, Loading instructions, conditional Execution, Assembly Programming.  Module:6 Thumb Instruction Set 6 hours  Thumb Instruction-Thumb Registers, ARM Thumb interworking, branch instruction, data processing instruction, single/multiple load store instruction, Stack instruction, SWI instruction, Assembly Programming.  Module:7 ARM Core based Microcontroller 8 hours  Architecture of LPC214X, Memory Addressing, IO ports, Timers/counter, Watch Dog Timer, PWM, ADC/DAC, UART, Interrupts, Displays, C programming.	Programming in C & Assembly for – Interrupts, Timers and Interfaces – PORTS, LED, ADC,								
ARM Design Philosophy; Overview of ARM architecture; States [ARM, Thumb, Jazelle]; Registers, Modes; Conditional Execution; Pipelining; Vector Tables; Exception handling.  Module:5   ARM Instruction Set   6 hours  ARM Instruction- data processing instructions, branch instructions, load store instructions, SWI instruction, Loading instructions, conditional Execution, Assembly Programming.  Module:6   Thumb Instruction Set   6 hours  Thumb Instruction-Thumb Registers, ARM Thumb interworking, branch instruction, data processing instruction, single/multiple load store instruction, Stack instruction, SWI instruction, Assembly Programming.  Module:7   ARM Core based Microcontroller   8 hours  Architecture of LPC214X, Memory Addressing, IO ports, Timers/counter, Watch Dog Timer, PWM, ADC/DAC, UART, Interrupts, Displays, C programming.	SENSORS	, LCD, DAC, Serial Communication							
Registers, Modes; Conditional Execution; Pipelining; Vector Tables; Exception handling.  Module:5   ARM Instruction Set   6 hours  ARM Instruction- data processing instructions, branch instructions, load store instructions, SWI instruction, Loading instructions, conditional Execution, Assembly Programming.  Module:6   Thumb Instruction Set   6 hours  Thumb Instruction-Thumb Registers, ARM Thumb interworking, branch instruction, data processing instruction, single/multiple load store instruction, Stack instruction, SWI instruction, Assembly Programming.  Module:7   ARM Core based Microcontroller   8 hours  Architecture of LPC214X, Memory Addressing, IO ports, Timers/counter, Watch Dog Timer, PWM, ADC/DAC, UART, Interrupts, Displays, C programming.	Module:4	ARM Architecture	4 hours						
Module:5ARM Instruction Set6 hoursARM Instruction- data processing instructions, branch instructions, load store instructions, SWI instruction, Loading instructions, conditional Execution, Assembly Programming.Module:6Thumb Instruction Set6 hoursThumb Instruction-Thumb Registers, ARM Thumb interworking, branch instruction, data processing instruction, single/multiple load store instruction, Stack instruction, SWI instruction, Assembly Programming.Module:7ARM Core based Microcontroller8 hoursArchitecture of LPC214X, Memory Addressing, IO ports, Timers/counter, Watch Dog Timer, PWM, ADC/DAC, UART, Interrupts, Displays, C programming.	ARM Desig	ARM Design Philosophy: Overview of ARM architecture: States [ARM, Thumb, Jazelle]:							
ARM Instruction- data processing instructions, branch instructions, load store instructions, SWI instruction, Loading instructions, conditional Execution, Assembly Programming.  Module:6 Thumb Instruction Set 6 hours  Thumb Instruction-Thumb Registers, ARM Thumb interworking, branch instruction, data processing instruction, single/multiple load store instruction, Stack instruction, SWI instruction, Assembly Programming.  Module:7 ARM Core based Microcontroller 8 hours  Architecture of LPC214X, Memory Addressing, IO ports, Timers/counter, Watch Dog Timer, PWM, ADC/DAC, UART, Interrupts, Displays, C programming.									
SWI instruction, Loading instructions, conditional Execution, Assembly Programming.  Module:6 Thumb Instruction Set 6 hours  Thumb Instruction-Thumb Registers, ARM Thumb interworking, branch instruction, data processing instruction, single/multiple load store instruction, Stack instruction, SWI instruction, Assembly Programming.  Module:7 ARM Core based Microcontroller 8 hours  Architecture of LPC214X, Memory Addressing, IO ports, Timers/counter, Watch Dog Timer, PWM, ADC/DAC, UART, Interrupts, Displays, C programming.	Module:5	ARM Instruction Set	6 hours						
Module:6Thumb Instruction Set6 hoursThumb Instruction-Thumb Registers, ARM Thumb interworking, branch instruction, data processing instruction, single/multiple load store instruction, Stack instruction, SWI instruction, Assembly Programming.Module:7ARM Core based Microcontroller8 hoursArchitecture of LPC214X, Memory Addressing, IO ports, Timers/counter, Watch Dog Timer, PWM, ADC/DAC, UART, Interrupts, Displays, C programming.	ARM Instru	uction- data processing instructions, branch instr	uctions, load store instructions,						
Thumb Instruction-Thumb Registers, ARM Thumb interworking, branch instruction, data processing instruction, single/multiple load store instruction, Stack instruction, SWI instruction, Assembly Programming.  Module:7   ARM Core based Microcontroller   8 hours  Architecture of LPC214X, Memory Addressing, IO ports, Timers/counter, Watch Dog Timer, PWM, ADC/DAC, UART, Interrupts, Displays, C programming.	SWI instruc	ction, Loading instructions, conditional Execution	, Assembly Programming.						
processing instruction, single/multiple load store instruction, Stack instruction, SWI instruction, Assembly Programming.  Module:7   ARM Core based Microcontroller   8 hours  Architecture of LPC214X, Memory Addressing, IO ports, Timers/counter, Watch Dog Timer, PWM, ADC/DAC, UART, Interrupts, Displays, C programming.	Module:6	Thumb Instruction Set	6 hours						
instruction, Assembly Programming.  Module:7 ARM Core based Microcontroller 8 hours  Architecture of LPC214X, Memory Addressing, IO ports, Timers/counter, Watch Dog Timer, PWM, ADC/DAC, UART, Interrupts, Displays, C programming.	Thumb Ins	struction-Thumb Registers, ARM Thumb interv	vorking, branch instruction, data						
Module:7ARM Core based Microcontroller8 hoursArchitecture of LPC214X, Memory Addressing, IO ports, Timers/counter, Watch Dog Timer, PWM, ADC/DAC, UART, Interrupts, Displays, C programming.	processing	instruction, single/multiple load store instruction	on, Stack instruction, SWI						
Architecture of LPC214X, Memory Addressing, IO ports, Timers/counter, Watch Dog Timer, PWM, ADC/DAC, UART, Interrupts, Displays, C programming.	instruction,	Assembly Programming.							
PWM, ADC/DAC, UART, Interrupts, Displays, C programming.	Module:7	ARM Core based Microcontroller	8 hours						
Module:8 Contemporary Issues 2 hours	PWM, ADO	C/DAC, UART, Interrupts, Displays, C programm	ing.						
	Module:8	Contemporary Issues	2 hours						
Total Lecture hours: 45 hours		Total Lecture hours:	45 hours						
Text Book(s)	Text Book	(s)							
1. Andrew N.Sloss, Dominic Symes, Chris Wright, ARM Developer's Guide, 2010, 1st									

2.	Kenneth Ayala, The 8051 Microcontroller & Embedded Systems Using Assembly and C, 2010, 1st edition, Cengage Learning, United States					
Re	Reference Books					
1.	1. Steve Furber ARM System on Chip Architecture, 2010, 2 <sup>nd</sup> Edition, Addison Wesley, United States					
2.	Technical Reference Manual CORTEX M-3, ARM, 2010, United States					
Мо	de of Evaluation: Continuous Asse	ssment, Digital	Assignme	ent, Quiz and Final		
Ass	sessment Test	_				
Re	commended by Board of Studies	28-07-2022				
App	Approved by Academic Council No. 67 Date 08-08-2022					

Course Code	Course Title		L T P C
MEDS502P	Microcontroller Architecture and Organization		0 0 2 1
Pre-requisite	NIL		s version .0
Course Objectiv	es		.0
The course is aim			
<ol> <li>Describing</li> <li>Teaching</li> <li>Designing other perip</li> <li>Solving re</li> <li>Solving re</li> <li>Teaching</li> <li>Solving re</li> <li>Develop A</li> <li>Develop A</li> <li>Develop A</li> <li>Develop A</li> <li>Develop A</li> </ol>	g the architecture of 8051 microcontroller and ARM prothe instruction set of 8051 and ARM microcontroller to system in block level using microcontroller, memory pheral devices al life problem using microcontroller-based systems are course the students will be able to assembly program applying Digital logic and mathemat assembly Language Program for ARM and ARM periphal with minimum instructions and memory.	efficient provided devices, devices, devices, devices, devices, devices device	buses and
time	and evaluate the given program in terms of code siz	e and con	nputational
Indicative Exper			
1 Task-1: Calcu	lator Application	7	7 hours
	sk 1: Make the LCD interfaced to 8051		
Sub ta	sk 2: Get input from switch which is interfaced to 8051	and	
	display it on LCD	_	
Sub ta Calcul	sk 3: Based on switch input, perform basic operation of	of a	
		-	7 hours
Sub ta	d control of motor ssk-1: Use timer and generate an exact time delay for <sup>-</sup>		nouis
	sk-2: Use timer interrupt in generating the waveform		
	st-3: Controlling speed of a DC motor using Timer		3 hours
Sub ta Sub Ta Sub Ta Sub ta Via Zig	controller based application usk-1: Interface Zigbee with 8051 ask-2: Interface keypad with 8051 ask-3: Interface GSM with 8051 sk-4: Based on KEY pressed in keypad, transmit the kaybee and make a motor to rotate, which is interfaced w	ey info ith 8051.	Jilouis
	GSM module send the status of motor[run/stop] to the		<u> </u>
Sub Ta Sub Ta Sub Ta Sub Ta	or interfacing with ARM LPC2148  ask-1: Interface IR with LPC2148  ask-2: Interface temperature sensor with LPC2148  ask-3: Interface Bluetooth with LPC2148  ask-4: Transmit the IR detail and sensor data to another  2148 via Bluetooth.		3 hours
LP U2	Total Laboratory	Hours 3	30 hours

Date

Mode of Assessment: Continuous Assessment and Final Assessment Test

No. 67

Recommended by Board of Studies | 28-07-2022

Approved by Academic Council

08-08-2022

Course Code	Course Title		LTPC
MEDS503L	Embedded Programmi	ng	3 0 0 3
Pre-requisite	NIL		Syllabus version
•			1.0
Course Objectiv	ves		
The course is ain	ned		
1. To acqua	int students with fundamentals of C		
<ol> <li>To familia</li> </ol>	rize the students with data structures		
<ol><li>To introdu</li></ol>	uce the students with SHELL programming	and Linux	
<ol><li>To Impler</li></ol>	ment the Device drivers in LINUX environm	ent	
Course Outcom	е		
At the end of the	course the students will be able to		
	end the fundamentals of C		
<ol><li>Compreh</li></ol>	end the Data structures		
-	end the basics of Linux		
	e the skill, knowledge and ability of SHELL		g.
	e working knowledge of basic Embedded		
	end the concepts of Kernel module Progra	mming	
	vice driver programs		
8. Have han	ds on experience in using state-of- art har	dware and so	ftware tools
		I	
	nguage	<u> </u>	7 hours
	of C, Embedded C Vs C, Embedded progra		
	Functions, Arrays, pointers, structures and	d Inputs/Outp	
	structures of kernel programming		6 hours
Module:3 Linu	e linked list, Double linked list and Queues	• 	C haura
		entara Circalira	6 hours
	pt, X windows basics, Navigating file sy		
	files text editing in Linux, Compression Management, I/O Handling, File Locking.	and archivin	g tools, basic shell
Module:4 Shel			7 hours
	g more than one command at a time, p	l orioritizina an	
	mands, pipes and redirection, regular ex		
	or while, if and other commands.	pression, pa	tterri matering,
	edded Linux		6 hours
	ooting process, make files, using SD card	and reader to	
	INUX system calls, API's, device drivers,		
driver.	intert eyetem eane, in ite, device anvere,	complining an	a motalling a device
	nel Module Programming		6 hours
	, Configuring Kernel and compilation, Kern	nel code, brov	
	of modules, User space, kernel space con		
Writing, Make-file	· · · · · · · · · · · · · · · · · · ·	[ ,	<b>3</b> • • • • • • • • • • • • • • • • • • •
<u> </u>	ce Driver concepts		5 hours
	Block & character driver distinction, Lo	w level drive	
	drivers, Device major, minor number.		,
<u>~</u>	temporary Issues		2 hours
l		•	
	Total Lecture hours:		45 hours

1. Neil Mathew, Richard stones, Beginning Linux Programming, 2012 reprint, Wrox – Wiley

Text Book(s)

Publishing, USA.

2.	2. Eric Foster Johnson, John C. Welch, Micah Anderson, Beginning shell scripting, 2012, reprint, Wrox – Wiley Publishing, USA					
Re	Reference Books					
1.	Derek Molloy, Exploring Beagle Bone: Tools and Techniques for Building with Embedded Linux, 2015, 1st Edition, Wiley Publications, USA					
	Mode of Evaluation: Continuous Assessment, Digital Assignment, Quiz and Final Assessment Test					
	commended by Board of Studies	28-07-2022				
Approved by Academic Council No. 67 Date 08-08-2022						

Course Code	Course Title		L	Т	Р	С
MEDS503P	Embedded Programming Lab		0	0	2	1
Pre-requisite	NIL	Syll	abı	IS V	ers	on
				1.0		

The course is aimed

- 1. To acquaint students with fundamentals of C
- 2. To familiarize the students with data structures
- 3. To introduce the students with SHELL programming and Linux
- 4. To Implement the Device drivers in LINUX environment

### **Course Outcome**

At the end of the course the students will be able to

- 1. Comprehend the fundamentals of C
- 2. Comprehend the Data structures
- 3. Comprehend the basics of Linux
- 4. Showcase the skill, knowledge and ability of SHELL programming.
- 5. Exhibit the working knowledge of basic Embedded Linux
- 6. Comprehend the concepts of Kernel module Programming
- 7. Write Device driver programs
- 8. Have hands on experience in using state-of- art hardware and software tools

Indi	cative Experiments					
1.	Task1: C programming				6 hours	
	<ul> <li>Implement a binary tree so</li> </ul>	orting				
	<ul> <li>Implement a dice throw ga</li> </ul>	ıme				
	Implement a command line argum	nent based app	lication of	automation		
2.	Task2: Implementation of data str	ucture for an a	oplication		6 hours	
	Write a SortedMerge() function th	at takes two lis	ts, each o	f which is		
	sorted in increasing order, and me	to one list				
	which is in increasing order. Sorte	edMerge() shou	ıld return t	the new list.		
	The new list should be made by s	plicing togethe	the node	s of the first		
	two lists.					
3.	Task3: Shell Programming				6 hours	
	Development of inventory manage	gement system	n using S	hell scripting		
	with the following features					
	<ul> <li>User may add/update/dele</li> </ul>	•				
	<ul> <li>User may add/update inve</li> </ul>					
	<ul> <li>Details include cost, quant</li> </ul>					
	Includes forms for inventory inwar		ds.			
4.	Task4: Build process for an embe				6 hours	
	Build a kernel for a Beagle Bone I			oard bring		
	up, kernel module program on an					
5.	Task5: Device driver programming	• •			6 hours	
				ratory Hours	30 hours	
	de of Assessment: Continuous Asse		nal Asses	sment Test		
	commended by Board of Studies	28-07-2022				
App	Approved by Academic Council No. 67 Date 08-08-2022					

Course Code	Course Title	L	T	Р	С
MEDS504L	In Vehicle Networking	3	0	0	3
Pre-requisite	NIL	Sylla	bus v	versi	on
			1.0	)	

The course aimed at

- 1. Providing students, a working knowledge of in-vehicle network systems
- 2. Giving exposure to aspects of design, development, application and performance issues associated with in vehicle networking systems.
- 3. Illustrating concepts of sensor data capture, storage and exchange of data to access remote services

### **Course Outcomes**

The students will be able to

- Know the need for In Vehicle Networking and the basics of data communication and networking concepts.
  - Comprehend the general protocols, CAN and their usage in automotive sector.
- 3. Have an overview of the CAN higher layer protocols like CAN open, Device Net, TTCAN and SAE J1939.
- 4. Understand the working mechanism of LIN protocol.
- 5. Get an overview of MOST protocol used in automotive for multimedia applications.
- 6. Comprehend protocols like FlexRay used in automotive for fault tolerant applications.

### Module:1 Concepts of In-vehicle networking Overview of Data communication and networking–need for In-Vehicle networking–layers of OSI reference model–multiplexing and de-multiplexing concepts–vehicle buses.

Module:2	General purpose protocols	7	hours	
Overview of	general-purpose networks and protocols -Ethernet	TCP,	UDP,	IP,
WiFi, Blueto	oth, NFC			

### Module:3 Networks and protocols 8 hours

CAN protocol: principles of data exchange-real time data transmission-message frame formats, bit encoding-bit-timing and synchronization-data rate and bus length-network topology-bus access- physical layer standards.

### Module:4 CAN higher layer protocol 6 hours

Introduction to CAN open –Device net–TTCAN–SAEJ1939–overview of CAN open and applications in transportation electronics–CAN open standards.

### Module:5 LIN protocol 5 hours

LIN standard overview – applications – LIN communication concept message frame–development flow.

Module:6	MOST	5 hours
MOST overv	riew-data rates-data types-topology -application area	S.

Module:7 FlexRay 6 hours

Flex Ray introduction-network topology-ECU sand bus interfaces-controller host interface and protocol operation controls-media access control and frame and

	symbol processing-coding/decoding unit-Flex Ray scheduling-message						
		wakeup/startup-application	ons.				
		Contemporary Topics				2 hours	
Gu	iest Lectu	res from Industry and, Res	search an	d Develo	pment Org	janizations	
			Tota	al Lectui	re hours:	45 hours	
Te	Text Book(s)						
1.	1. Dominique Paret, Multiplexed Networks for Embedded Systems CAN, LIN,						
	FlexRay	, Safeby-Wire, 2014, 1 <sup>st</sup> ed	lition, Wile	y, United	d States.		
Re	ference	Books					
1.		<i>I</i> ling Huang, YuhShyan Ch					
	and Ve	ehicular Networks: Wirel	ess Arch	itectures	and Ap	plication, 2010,	
	1 <sup>st</sup> editio	n, Information Science Ref	ference, L	Inited St	ates.		
2.		K Jurgen, Distributed Auto	motive En	nbedded	Systems,	2010, 4 <sup>th</sup> Edition,	
	SAE Inte	ernational, United States.					
3.		Zurawski, Industrial Co		ion Tec	hnology H	landbook, 2015,	
	2 <sup>nd</sup> Editio	on, CRC press, United Sta	tes.				
4.		Reif, Automotive Mechatroi					
	Systems	s Electronics, 2015, 2 <sup>nd</sup> Edi	tion, Sprir	iger, Uni	ted States.		
Mc	de of Ev	aluation: Continuous Asse	essment,	Digital A	ssignment,	, Quiz and Final	
	sessmen						
		ded by Board of Studies	07-06-20				
Ар	Approved by Academic Council No. 70 Date 24-06-2023						

Course Code	Course Title			Т	Р	С
MEDS505L	Real Time Operating System		3	0	0	3
Pre-requisite	NIL	Syll	abu	IS V	ersi	on
				1.0		

The course is aimed at

- 1. Introducing the students about Operating Systems and acquainting students to Real Time Operating Systems
- 2. Teaching the students about Task Management and Enabling students to understand RTOS Scheduling
- 3. Introducing the students about interprocess communication and Memory Management

### **Course Outcome**

At the end of the course the will should be able to

- 1. Comprehend the basic components of an operating system
- 2. Learn about the basics of real-time concepts
- 3. Acquire knowledge about task management
- 4. Acquaint with RTOS scheduling
- 5. Learn about IPC synchronization
- 6. Learn about IPC data exchange
- 7. Perform memory management in RTOS
- 8. Apply the knowledge for developing practical applications of modern real-time systems.

Module:1	Introduction to Operating Systems	6 hours
Layers of	Operating Systems, Operating systems functions	s, System Boot up - BIOS & Boot
	Kernel – Monolithic and Microkernel	
Module:2	Real Time Operating Systems	7 hours
	for RTOS, POSIX	
	Task Management	7 hours
	nd Threads, Process Control Block, Process Attri	butes, POSIX Threads
	RTOS Scheduling	7 hours
Priority ba	sed scheduling, Rate-Monotonic scheduling, Earl	liest Deadline first scheduling,
Linux RT		
Module:5	IPC - Synchronization	7 hours
	e conditions and critical sections, Signals, Atomic	c operations, Semaphore, Mutex,
	Priority Inversion and Priority ceiling.	
	IPC – Data Exchange	7 hours
	emory, FIFO, Messages and Mailbox, Circular an	
	Memory Management	2 hours
	lanagement, shared memory	
Module:8	Contemporary Issues	2 hours
	Total Lecture hours:	45 hours
Text Boo	((s)	
	κ(s) a K., Real Time Systems, Design for distributed	Embedded Applications, 2011,
1. Herm	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	Embedded Applications, 2011,
1. Herm 2 <sup>nd</sup> ec	a K., Real Time Systems, Design for distributed	• •
1. Herm 2 <sup>nd</sup> ecc 2. Taner Hall, I	a K., Real Time Systems, Design for distributed ition, Springer, USA.  baum, Andrew, Modern Operating Systems, 20  JSA	• •
1. Herm 2 <sup>nd</sup> ecc 2. Taner	a K., Real Time Systems, Design for distributed ition, Springer, USA.  baum, Andrew, Modern Operating Systems, 20  JSA	• •
1. Herm 2 <sup>nd</sup> ecc 2. Taner Hall, I	a K., Real Time Systems, Design for distributed ition, Springer, USA.  baum, Andrew, Modern Operating Systems, 20  JSA	015, 4 <sup>th</sup> ed.,, Pearson Prentice
1. Herm 2 <sup>nd</sup> ecc 2. Taner Hall, I Reference 1. Ivan Embe	a K., Real Time Systems, Design for distributed ition, Springer, USA.  baum, Andrew, Modern Operating Systems, 20  JSA  Books	015, 4 <sup>th</sup> ed.,, Pearson Prentice briele Manduchi, Real-Time

2.	Lyla B. Das, Embedded Systems an Integrated Approach, 2012, 1 <sup>st</sup> ed., Pearson Education, India.							
	Mode of Evaluation: Continuous Assessment, Digital Assignment, Quiz and Final Assessment Test							
Recommended by Board of Studies 28-07-2022								
Apı	proved by Academic Council	No. 67	Date	08-08-2022				

Course Code	Course Title		L	Т	Р	С
MEDS505P	MEDS505P Real Time Operating System Lab		0	0	2	1
Pre-requisite	NIL	Syllabus versio			ion	
		1.0				

The course is aimed at

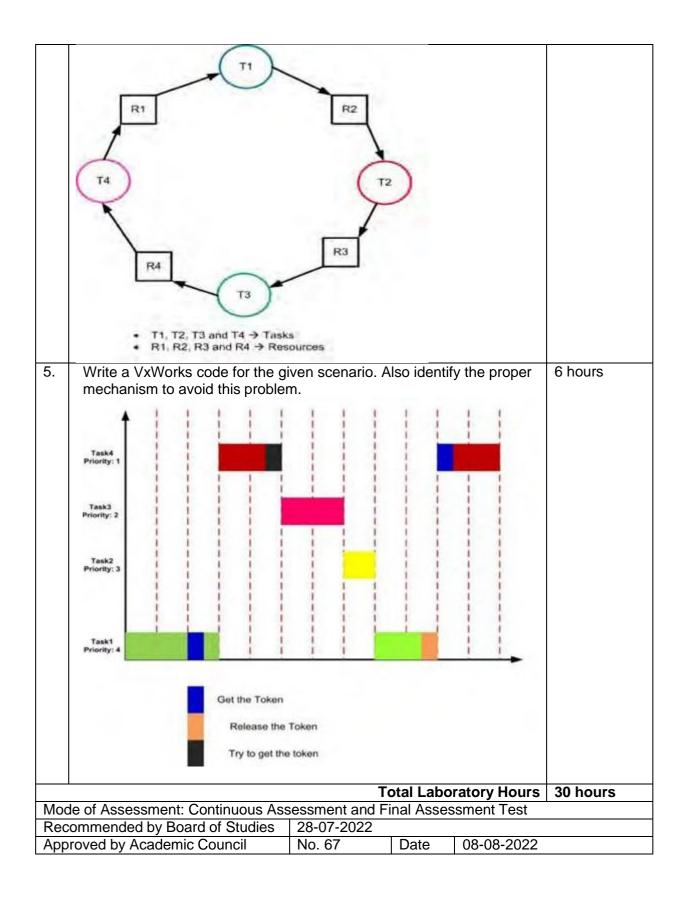
- 1. Introducing the students about Operating Systems and acquainting students to Real Time Operating Systems
- 2. Teaching the students about Task Management and Enabling students to understand RTOS Scheduling
- 3. Introducing the students about interprocess communication and Memory Management

### **Course Outcome**

At the end of the course the will should be able to

- 1. Comprehend the basic components of an operating system
- 2. Learn about the basics of real-time concepts
- 3. Acquire knowledge about task management
- 4. Acquaint with RTOS scheduling
- 5. Learn about IPC synchronization
- 6. Learn about IPC data exchange
- 7. Perform memory management in RTOS
- 8. Apply the knowledge for developing practical applications of modern real-time systems.

lua cl!	active Everylments	
	cative Experiments	
1.	Write a C code for a simple calculator (+, -, *, /) using functional	6 hours
	pointer as argument in a function	
	int add (int x, int y)	
	int sub (int x, int y)	
	intmul (int x, int y)	
	int div (int x, int y)	
	int (*mathop)(int, int)	
	intdomath(int (*mathop)(int , int), int x, int y)	
2.	Write a program to create multiple threads carrying out different	6 hours
	functions.	
	Thread 1: Accepting a string from the user.	
	Thread 2: Display the string in upper case.	
	Thread 3: Count the number of vowels in the string	
	Thread 4: Count the number of special characters in the string.	
3.	Write a program to create three threads, which are implemented using	6 hours
	function pointers. First thread is for getting a list of numbers from the	
	keyboard, second thread is helpful to extract the ODD and EVEN list	
	from the given list, and the third one is used to arrange the ODD and	
	EVEN list of numbers in an order. Use Mutex semaphore.	
	Note:	
	First Thread for getting input data from keyboard.	
	Second Thread to identify the ODD and EVEN list	
	Third Thread to get descending ordered ODD list	
	Fourth Thread to get ascending ordered EVEN list	
	Input data: 56, 23, 12, 64, 87, 02, 45, 88, 35, 67.	
4.	Write a Vx Works code for the given scenario. Also identify the proper	6 hours
	mechanism to avoid this problem.	



Course Code	Course Title		LTPC
MEDS506L	Wireless and Mobile Commu	nication	3 0 0 3
Pre-requisite	NIL	Sy	llabus version
			1.0
Course Objective			
The course aime			
	out wireless mobile communication syster		and
2. To keep ab	reast of the future of mobile communication	n	
0			
Course Outcom			
The students will			
	ced Cellular Mobile Communication system		
	d and solve telecommunication design is	sues using cellula	ar and trunking
theory.	e effect of multipath channels and sugge	et a cuitable mad	al for indoor or
outdoor ap		st a sultable filou	ei ioi iliuooi oi
•	te the implications of multipath parameters	in mobile commur	nication
	e Channel coding for Mobile Radio		noation.
	e Modulation techniques for Mobile Radio		
7. Get introdu	ced to Advanced Communication Systems	and Wireless Star	ndards
	,		
Module:1 Cell	ular Mobile Systems		4 hours
Cellular Mobile (	Communication Evolution - Types of mobil	e wireless services	s/systems – 1G
& 2G Mobile Cor	nmunication Technology		
Module:2 Cell	ular Concept		7 hours
	- Frequency reuse - Channel assignment		
	system capacity - Trunking & Grade of s	ervice – Improvinç	g coverage and
capacity in cellula		1	
	ile Radio Propagation	<u> </u>	9 hours
	pagation Model – Basic Propagation n		
	Ray) model – Outdoor Propagation Model	s: Okumura Mode	i, Hata Model –
	on Model: Attenuation Factor Model.  II Scale Propagation models		4 hours
		ocala fadina Fad	
	obile multipath channels – Types of small delay spread and Doppler spread	scale lading – Fad	ing effects due
	rmation Theory and Coding		6 hours
	entropy - Coding of memoryless sources:	l Shannon-Fano / H	
	emory: Markov model – Source Coding: Li		
	hannel Coding: Convolutional coding, Viter		
	iplexing & Modulation Schemes		6 hours
	FIFO, Messages and Mailbox, Circular an	d swinging buffers	
	anced Communication Systems and		7 hours
	eless Standards		
3G, 4G and 5G	and beyond wireless standards - WLAN A	Architecture design	and WIMAX -
VANETS	•		
Module:8 Con	temporary Issues		2 hours
	Total Lecture hours:		45 hours
Text Book(s)		I	
<u>`</u>	aupt, Wireless Communications Systems:	An Introduction. V	Viley-IEEE
Press, Janua	• •		-, - <u></u>
	ort, Wireless Communication -Principle and	d Practice ,Prentice	e Hall, 2010.
Reference Book			

Reference Books

1.	W.C.Y.Lee, Wireless and Cellular Communication, McGraw Hill, 2006							
2.	2. Schiller, Mobile Communications; Pearson Education Asia Ltd., 2008							
	Mode of Evaluation: Continuous Assessment, Digital Assignment, Quiz and Final Assessment Test							
	Recommended by Board of Studies 28-07-2022							
Apı	proved by Academic Council	No. 67	Date	08-08-2022				

Course Code	Code Course Title		L	T	Р	С
MEDS507L	DS507L Electronic Hardware System Design		2	0	0	2
Pre-requisite	NIL	Syllabus version			ion	
		1.0				

The course is aimed at

- 1. Emphasing students the significant role of FPGA in System design and development.
- 2. Teaching the students to develop program using Hardware Descriptive Language and model digital logic combinational and sequential circuits.
- 3. Enabling the students acquire knowledge in Interfacing peripherals, Board Design, Packaging, PCB Design and Analysis
- 4. Motivating students to solve real life problem using FPGA based systems.

### **Course Outcome**

At the end of the course the student will be able to

- 1. Comprehend the architecture of FPGA and design flow
- 2. Understand Hardware Description Language
- 3. Design and develop combinational logic circuits using Verilog and VHDL program.
- 4. Design and develop sequential logic circuits using Verilog and VHDL program.
- 5. Interface peripherals with FPGA.
- 6. Design the PCB
- 7. Design FPGA based system
- 8. Comprehend upcoming trends in FPGA.

### Module:1 | Programmable Logic Devices & FPGAs 4 hours Introduction to FPGAs. FPGA technologies. FPGA Architectures [Xilinx. Altera. ACTEL. LATTICE], FPGA Design Flow Prototyping with Xilinx FPGAs, FPGA based Testing. Module: 2 | Hardware Descriptive Language 3 hours (Verilog/VHDL) Cellular concept – Frequency reuse – Channel assignment strategies – Handoff strategies - Interference & system capacity - Trunking & Grade of service - Improving coverage and

capacity in cellular system.

### Module:3 | Modeling of Combinational logic circuits

3 hours

Free Space Propagation Model - Basic Propagation mechanism - Two Ray Ground Reflection (Two Ray) model - Outdoor Propagation Models: Okumura Model, Hata Model -Indoor Propagation Model: Attenuation Factor Model.

### Module:4 | Modeling of Sequential logic circuits

4 hours

Flip Flops-Realization of Shift Register -Realization of a Counter-Synchronous and Asynchronous – BCD counter, Mealy and Moore State Machines, Sequence detector, FIFO, Memory Design, Serial Data Receiver, Serial to parallel data converter.

### Module:5 Interfacing peripherals and Board Design

5 hours

Interfacing to 7 segment display, Stepper Motor, ADC and Sensors, FPGA System Architecture, Constraints -Logical -Electrical -Physical, Power distribution for FPGAs, Clock design, I/O buses

### Module:6 Introduction to Packaging &PCB Design

Physical integration of circuits, packages, boards and full electronic systems - Package classifications (Through hole and SMDs) and packaging trends, Hierarchy of Interconnection Levels -Signal integrity - The PCB Design Process - Defining the Layout Cross Section -Design Rules Checking - Working with Properties & Constraints- PCB Electrical Design Consideration - Design tips for Placement / Fan-out and Wiring - Multi - Layer Design Issues.

### Module:7 | High Speed PCB design and Analysis **Wireless Standards**

5 hours

High speed PCB design -EMI/EMC analysis - Thermal management of electronic devices and systems -Thermal interface material, Cooling mechanisms-System level design of electronic hardware for automotive applications -System level testing and validation of

	automotive electronics systems for reliability. Layout constraints for FPGAs, FPGA-based PCB schematics.								
		Contemporary Issues			2 hours				
				•					
		T	otal Lecture ho	ours:	30 hours				
Tex	kt Book	(s)							
1.		Monk, Make Your Own Poed Boards, 2014, First Edition							
2.	Wayne	Wolf, FPGA-based Syster	n Design, 2011,	Re-Print	, Prentice Hall, India				
Ref	ference	Books							
1.	•	Coombs, Printed Circuits F sional, USA	landbook, 2011	, Sixth Ed	dition, McGraw Hill				
2.	lan Gr UK.	out, Digital Systems, Desig	gn with FPGAs	and CPLI	Ds, 2012, Re-Print, Newness,				
3.		Ronald R. Sass and Andrew Schmidt, Embedded Systems Design with Platform FPGAs: Principles and Practices, 2010, First Edition, Morgan Kaufman Publishers, USA.							
	de of Ev sessmer	valuation: Continuous Asse nt Test	ssment, Digital	Assignme	ent, Quiz and Final				
Red	commer	nded by Board of Studies	28-07-2022						
App	oroved b	y Academic Council	No. 67						

Course Code	Course Title		L	T	Р	С
MEDS507P	Electronic Hardware System Design Lab				2	1
Pre-requisite	NIL	Syllabus version		on		
		1.0				

The course is aimed at

- 1. Emphasing students the significant role of FPGA in System design and development.
- 2. Teaching the students to develop program using Hardware Descriptive Language and model digital logic combinational and sequential circuits.
- 3. Enabling the students acquire knowledge in Interfacing peripherals, Board Design, Packaging, PCB Design and Analysis
- 4. Motivating students to solve real life problem using FPGA based systems.

### **Course Outcome**

At the end of the course the student will be able to

- 1. Understand Hardware Description Language
- 2. Design and develop combinational logic circuits using Verilog and VHDL program.
- 3. Design and develop sequential logic circuits using Verilog and VHDL program.
- 4. Interface peripherals with FPGA.

	Indi	cative Experin	nents					
1.	Task 1: Combination Logic:-				8 hours			
	Design a 16-bit microprocessor	that is capab	le of perf	forming both				
	logical and arithmetic operation.							
2.	Task 2: Sequential Logic:-				8 hours			
	Design a controller for vending m	achine which s	ells cand	y bars for Rs				
	5, 10 and 20.							
3.	Task 3: Peripheral Interfacing:-				8 hours			
	Design a car speed monitor us							
	segment display (b) LEDs (c) S	•		` ,				
	Buzzer. The cars electronic sp	•		•				
	whose frequency is proportional t							
	of the design use function generator to provide the speedometer clock.							
4.	Task 4:PCB Design:-				6 hours			
	Design a PCB for a circuit with a	a mixture of ar	nalog and	digital parts,				
	multiple power planes, and a sing		•	•				
	digital sections that have a comm	on reference p	oint using	open source				
	30 hours							
	de of Assessment: Continuous Asse	•	nal Asses	sment Test				
	commended by Board of Studies	28-07-2022						
App	roved by Academic Council	No. 67	Date	08-08-2022				

Course Code	Course Title	L	Т	Р	С
MEDS601L Electromagnetic Interference and Compatibility		3	0	0	3
Pre-requisite	NIL	Syllabus version			ion
•		1.0			

The course is aimed at:

- 1. Imparting knowledge about EMI environment
- Teaching EMI coupling principles, EMI control techniques and design of PCBs for EMC
- 3. Giving exposure to EMI Standards, Regulations and Measurements

### **Course Outcomes**

At the end of the course, the student will be able to

- 1. Understand terminologies of EMI and EMC
- 2. Analyze and understand various EMI coupling mechanisms
- 3. List various EMI Test and Measurement methods
- 4. Analyze various techniques needed to suppress EMI
- 5. Perceive different EMC regulations followed worldwide
- 6. Ability to design an Electromagnetic Compatible systems.
- 7. Analyze and comprehend different techniques needed for Signal Integrity and ability to understand various models for EMI/EMC

## Module:1EMI Environment4 hoursEMI-EMC Definitions and units of Parameters, Sources of EMI, conducted and radiated EMI, Transient EMIModule:2EMI Coupling Mechanisms6 hours

Conducted, Radiated and Transient Coupling, Common Impedance Ground Coupling, Radiated Common Mode and Ground Loop Coupling, Radiated Differential Mode Coupling, Near Field Cable to Cable Coupling, Power Mains and Power Supply Coupling.

### Module:3 EMI Test and Measurements 8 hours

EMI Specification / Standards / Limits: Units of specifications, Civilian standards Military standards. EMI Test Instruments / Systems, EMI Test, EMI Shielded Chamber, Open Area Test Site, TEM Cell Antennas, Conductors Sensors/Injectors/Couplers. EMI Measurement Methods: Military Test Method and Procedures, Calibration Procedures, Modeling interferences

Module:4 EMI Control Techniques 7 hours

Shielding, Filtering, Grounding, Bonding, Isolation Transformer, Transient Suppressors, Cable Routing, Signal Control, Component Selection and Mounting, Electrostatic discharge protection schemes

Module:5 | EMC Standards and Regulations | 5 hours |
National and Intentional standardizing organizations- FCC, CISPR, ANSI, DOD, IEC, CENEEC, FCC CE and RE standards, CISPR, CE and RE Standards, IEC/EN, CS standards, SAE Automotive EMC standard, Frequency assignment - spectrum

conversation.

Module:6 | System Design for EMC

8 hours

PCB Traces Cross Talk, Impedance Control, Power Distribution Decoupling, Zoning, Motherboard Designs and Propagation Delay Performance Models,

	System Enclosures, Power line filter placement, Interconnection and Number of						
Pri	nted Cir	cuit Boards, PCB and sub	system o	decouplii	ng		
Мо	dule:7	Signal Integrity and EMI	/EMC Mo	dels		5 hours	
Effe	ect of te	rminations on line wave f	orms, Ma	tching so	chemes	for Signal Integrity,	
Effe	ects of li	ne discontinuities, Statistic	al EMI/EI	VIC mode	els.		
Mo	dule:8	Contemporary Issues				2 hours	
Gu	est Lectu	ires from Industry and, Res	search and	d Develo	pment C	Organizations	
			Total I	_ecture	hours:	30 hours	
Tex	xt Book	(s)					
1.	Clayton	R. Paul,Introductiont	nFlectror	nagnetic	compat	nd tibility.2010. 2	
	,	, Wiley & Sons, New Jers		nagnetic	oompa	115111ty, 2010, 2	
Rei	ference	<u> </u>					
1.		/.ott, Electromagnetic Co	mpatibility	v Engine	ooring	2011 1stad John	
١.			ırıpatıbılıt	y Engine	eening,	ZOTT, TSIEG. JOHN	
2	,	nd Sons, NewJersey.		. N. A.L T.		0 11 1 6	
۷.		G. André and Kenneth					
	Produc	t Designers 2014, 1st ed.,	SciTech F	Publishin	g, New.	Jersey	
Mo	de of Ev	aluation: Continuous Asse	ssment, [	Digital As	ssignmei	nt, Quiz and Final	
Ass	sessmer	t Test					
Red	commen	ded by Board of Studies	07-06-20	)23			
App	proved b	y Academic Council	No. 70	Date	24-06-	2023	

Course Code	Course Title		L	Т	Р	С
MEDS602L	DS602L Advanced Digital Image Processing				0	3
Pre-requisite	NIL	Syllabus version			on	
		1.0				

The course is aimed at:

- 1. Revising the basics of digital image processing namely; image acquisition, digitizing, enhancing images in spatial domain, image transforms and enhancing images in frequency domain.
- 2. Enabling the students to acquire knowledge in image restoration, image compression, image segmentation and object recognition.
- 3. Motivating the students to apply image processing and classification algorithms for solving real life problems and introducing students to upcoming trends in Computer Vision.

### **Course Outcome**

At the end of the course, the student will be able to

- 1. Comprehend the image acquisition, digitization, and processing in spatial domain.
- 2. Understand algorithms and programs for processing an image in transform domain
- 3. Acquaint with the image enhancement and restoration techniques
- 4. Implement different compression techniques to compress an image
- 5. Adopt different segmentation and image representation techniques for image processing.
- 6. Understand the pattern recognition approaches for implementing the visual system.
- 7. Identify computer vision techniques in various real-time applications.

## Module:1Image Processing in Spatial Domain7 hoursFundamental steps in DIP – Elements of visual perception - Image Sampling and Quantization<br/>- Basic relationship between pixels. Image enhancement - Spatial Domain: Basic Grey level<br/>Transformations – Histogram Processing – Smoothing spatial filters- Sharpening spatial filters.<br/>Colour image Processing: Models, TransformationModule:2Image Transforms6 hours

Image Transforms: Two dimensional Fourier Transform- Discrete cosine transform - Multi-resolution analysis – Haar Transform- Discrete Wavelet Transform. Karhunen – Loeve transform. and SVD

Module:3	Frequency domain filtering and Image	6 hours
	Restoration	

Smoothing frequency domain filters- sharpening frequency domain filters- Homomorphic filtering.

Image Restoration: Image deformation and geometric transformations, Restoration techniques, Noise characterization, Linear, Position invariant degradations, Adaptive filters.

Module:4 Image Compression 6 hours

Image Compression Techniques - Lossy and Lossless compression- Entropy Encoding-JPEG and MPEG standards

### Module:5 Image Segmentation 7 hours

Detection of discontinuities – point, corner, edge detection- thresholding -edge based segmentation-region based segmentation- morphological segmentation - watershed algorithm Descriptors: Boundary descriptors-Region descriptors- Texture descriptors, RANSAC.

Module:6 Recognition and Classification		7 hours
Patterns a	nd pattern classes – Introduction to classification	n – Decision theoretic methods –

structural and syntactic classifiers - Clustering techniques - similarity measures hierarchical methods – K-Means algorithm – Cluster evaluation methods. Convolution neural networks, Region-based CNN, fully convolution networks, Multi-modal networks, Hybrid learning methods. Module:7 | Computer Vision Applications Face recognition application: personal photo collections – Instance recognition application: Location recognition - Machine learning applications: Deep voting, transfer learning and structured regression for image analysis and categorization. Module:8 | Contemporary Issues 2 hours Total Lecture hours: 45 hours Text Book(s) Rafael C. Gonzalez & Richard E. Woods, "Digital Image Processing", 4th Edition, 2018, David A. Forsyth and Jean Ponce, "Computer Vision: A Modern Approach", 2ndEdition, 2012, Prentice Hall, Pearson Education **Reference Books** Richard Szeliski, "Computer vision: Algorithm and Applications", Springer- Verlag, London, 2010. K. Jain, Fundamentals of Digital Image Processing, 2015, 3rd Edition, Pearson Education, USA. K.P.Soman, K.I. Ramchandran, N.G.Resmi, Insights into Wavelets, From Theory to Practice, 2013, 3rd Edition, PHI Learning Private Limited, New Delhi, India. Mark Nixon & Alberto Aguado, Feature Extraction, and Image Processing, 2013, 3rd Edition, Elsevier's Science & Technology Publications, USA William K. Pratt, Digital Image Processing, 2013, John Wiley & Sons, USA. Mode of Evaluation: Continuous Assessment, Digital Assignment, Quiz and Final Assessment Test Recommended by Board of Studies 28-07-2022 Approved by Academic Council No. 67 Date 08-08-2022

Course Code	Course Code Course Title			T	Р	С
MEDS603L Design and Analysis of Algorithms		3	0	0	3	
Pre-requisite NIL S		Syll	abı	IS V	ers	ion
				1.0		

This course is aimed at

- 1. Enabling the students to carry out analysis of various algorithms for mainly time and space complexity.
- 2. Teaching the students how to decide the appropriate data type and data structure for a given problem.
- 3. Teaching the students how to select the best algorithm to solve a problem by considering various problem characteristics, such as the data size, the type of operations, etc.

### **Course Outcome**

At the end of the course the student will be able to

- 1. Develop proficiency in problem solving and programming.
- 2. Comprehend Combinatorial Optimization
- 3. Analyse various algorithms for mainly time and space complexity.
- 4. Comprehend Cryptographic Algorithms
- 5. Learn Geometric Algorithms
- 6. Analyse Parallel Algorithms
- 7. Analyse and evaluate the given program in terms of code size and computational time.
- 8. Select the best algorithm to solve a problem by considering various problem characteristics, such as the data size, the type of operations, etc.

### Module:1 Introduction 7 hours Role of Algorithms in computing, Analysis of Algorithms, Asymptotic notation, Euclid's algorithm, Problem, Instance, RAM model, Principles of Algorithm Design, Sorting Algorithm - Insertion Sort & Complexity Analysis, Divide and Conquer Technique, Solving recurrences - substitution, Iteration, Recursion tree, Changing variable and Master's Method. Module:2 | Combinatorial Optimization 5 hours Backtracking; Dynamic programming; Greedy Technique; Branch & Bound Module:3 Advanced Algorithmic Analysis 5 hours Amortized analvsis: Online and offline algorithms; Randomized algorithms, **NP Completeness** Module:4 | Cryptographic Algorithms 9 hours Historical overview of cryptography; Private-key cryptography and the key-exchange problem; Public-key cryptography; Digital signatures; Security protocols; Applications (zero-knowledge proofs, authentication etc... Module:5 | Geometric Algorithms 7 hours Line segments: properties, intersections; convex hull finding algorithms, Voronoi Diagram, **Delaunay Triangulation** Module:6 Parallel Algorithms 5 hours PRAM model; Exclusive versus concurrent reads and writes; Pointer jumping; Brent's theorem and work efficiency. Module:7 RNNs, Auto encoders and GANs 5 hours Consensus and election; Termination detection; Fault tolerance; Stabilization; Module:8 | Contemporary Issues 2 hours **Total Lecture hours:** 45 hours Text Book(s)

1.	Anany Levitin, "Introduction to the Design and Analysis of Algorithms". 3rd edition.,2011, Addison Wesley, 2011					
2.	Cormen, Leiserson, Rivest and Stein , "Introduction to Algorithms", 3rd edition, McGraw-Hill, 2009					
Ref	ference Books					
1.	Ellis Horowitz, "Fundamentals of Computer Algorithms", 2nd Edition, Universities Press, 2008					
2.	M. J. Quinn, Parallel computing – t	heory and prac	ctice, McG	Graw Hill, 2002		
3.	Sukumar Ghosh, "Distributed Systems: An Algorithmic Approach",1st edition, Chapman & Hall/CRC Computer & Information Science Series, 2006					
4.						
Мо	Mode of Evaluation: Continuous Assessment, Digital Assignment, Quiz and Final					
Ass	Assessment Test					
	Recommended by Board of Studies 28-07-2022					
App	Approved by Academic Council No. 67 Date 08-08-2022					

Course Code	Course Title	L	Т	Р	С
MEDS605L	Hardware Software Co-design	2	0	0	2
Pre-requisite	NIL		Syll	abus v	ersion
				1.0	

The course is aimed at

- 1. Providing adequate knowledge in the modeling of heterogeneous embedded systems based on design constraint and provide alternate solution exploring trade-off.
- 2. Introducing the importance of estimating the cost analysis in terms of hardware and software parameters.
- 3. Introducing various co-synthesis and co-simulation tools for the effective design of embedded systems with better communication between different modules.

### **Course Outcome**

At the end of the course, the Students will be able to

- 1. Apply different MOCs based on system design specification.
- 2. Propose an alternate design solution based on constraint analysis.
- 3. Identify the partitioning solution based on the algorithms.
- 4. Understand various co-synthesis approaches.
- 5. Ability to pre-estimate and estimate the performance metrics for hardware and software based on cost analysis.
- 6. Approximate the pre-estimate and estimate the performance metrics for software based cost analysis.
- 7. Decide on proper co-simulation method based on system specification.

Module:1	Specification of embedded systems	4 hours					
Introduction	n to Co-design - Comparison of co	o-design approaches – Unified representation-					
Model-Mo0	Cs: State oriented, Activity oriented	d, Structure oriented, Data oriented and					
Heterogene	eous –Software CFSMs–Processor	Characterization.					
Module:2	HW/SW partitioning	4 hours					
	Constraints & tradeoffs						
	eling, Principle of hardware / softwn & constraints on Embedded syste	are mapping - Real time scheduling - design ems -Tradeoffs					
Module:3	HW/SW partitioning	4 hours					
	methodologies						
Partitioning	- Types of partitioning - Partition	on in granularity – Kernigan -Lin Algorithm-					
Extended F	Partitioning – Binary Partitioning: GC	CLP Algorithm					
Module:4	Co-synthesis	4 hours					
Software sy	Software synthesis – Hardware Synthesis- Interface Synthesis – Co-synthesis Approaches:						
Vulcan, Co	syma, Cosmos, Polis and COOL.						
Module:5	Estimation: Hardware	4 hours					
	area, execution timing and power, C						
	Estimation: Software	4 hours					
Software m	emory and execution timing, Worst	Case Execution Time, Case studies					
Module:7	Co-simulation & Co- verification	4 hours					
Principles of	of Co-simulation – Abstract Level;	Detailed Level – Co-Simulation as Partitioning					
support – C	support – Co- simulation using Ptolemy approach, Virtual Prototyping, Rapid Prototyping.						
Module:8	Contemporary Issues	2 hours					
	Total Lecture hours:	30 hours					

Te	Text Book(s)						
1	Soonhoi Ha, Jürgen Teich, "Han	dbook of Ha	rdware/Software	Co-design",			
	Springer, 2017						
Re	eference Books						
1	Schaumont, Patrick, A," A Practical	I Introduction t	o Hardware/Softv	ware Codesign",			
	2013, reprint, Springer, India.						
2	FeliceBalarin, Massimiliano Chiodo,	, Paolo Giusto	, Harry Hsieh,	Attila Jurecska,			
	Luciano Lavagno, Claudio Passero	one, Alberto S	Sangiovanni - V	/incentelli, Ellen			
	Sentovich, Kei Suzuki, BassamTabba	ara, "Hardware-	Software Co-Des	ign of Embedded			
	Systems: The POLIS Approach", Spr	ringer, 2012.					
3	http://ptolemy.eecs.berkeley.edu/ptole	emyll/ptll10.0/p	tll10.0.1_2014121	17/ptolemy/domai			
	. ns/continuous/doc/index.htm						
Mo	Mode of Evaluation: Continuous Assessment, Digital Assignment, Quiz and Final						
Assessment Test							
Re	Recommended by Board of Studies 28-07-2022						
Αp	Approved by Academic Council No. 67 Date 08-08-2022						

Course Code	Course Title			T	Р	С
MEDS606L	Modern Automotive Electronics Systems		3	0	0	3
Pre-requisite	NIL	Sylla	bu	s ve	ersi	on
			1	1.0		

The course is aimed at

- 1. Instilling fundamental understanding of various automatic control systems and basic instrumentation involved in automobiles.
- 2. Learning various automobile condition measurement and monitoring mechanisms.
- 3. Acquire with advanced electronic elements and their functional aspects in automobiles

### **Course Outcome**

Text Book(s)

At the end of the course the student will be able to

- 1. Comprehend engine management system.
- 2. Understand the various Ignition and Injection systems
- 3. Explain the automotive control mechanisms.
- 4. Learn the different monitoring systems for automobiles
- 5. Understand the typical sensors for transportation.
- 6. Acquire knowledge about upcoming trends in automotive electronics systems
- 7. Use the knowledge attained and develop appropriate systems for societal issues

### Module:1 | Engine management systems 8 hours Introduction - components for engine management system - Open loop and closed loop control system - Engine cranking and warm up control -Acceleration, deceleration and idle speed control. Module:2 Injection and ignition systems Feedback carburetor system-Throttle body injection and multi point fuel injection system-Injection system controls -Advantage of electronic ignition systems-Types of solid state ignition systems and their principles of operation -Electronic spark timing control, Exhaust emission control engineering Module:3 | Automotive control mechanism Electronic management of chassis systems, Vehicle motion control, anti - lock braking system, Tyre pressure monitoring system, Collision avoidance system, Traction control system. Module:4 | Automotive Electronics systems 6 hours Active suspension system Keyless entry system and Electronic power steering system, Electronic controls - lighting design - Horn - Warning systems - Brake actuation warning systems, Infotainment Module:5 | Monitoring of Automotive systems 6 hours Speed warning systems, oil pressure warning system, engine over heat warning system, air pressure warning system, safety devices-Wind shield wiper and washer, VANET Module:6 Sensors for transportation - I 5 hours Basic sensor arrangement-Types of sensors, Oxygen Sensor -Cranking Sensor -Position Sensors Module:7 | Sensors for transportation - II 4 hours Engine cooling water temperature Sensor-Engine oil pressure Sensor-Fuel metering -Vehicle speed sensor and detonation sensor. Module:8 | Contemporary Issues 2 hours **Total Lecture hours:** 45 hours

Tom Denton, Automobile Electrical and Electronic Systems, 2012, 4th Edition,

	Butter Worth Heinemann, United States					
2.	Bosch Automotive Electrics and Automotive Electronics, 2014, 5th Edition, Springer					
	Vieweg, United States					
3.	Beckwith, T.G, Roy D.Marangoni,	John H.Lien	hard, Me	chanical Measurements,		
	2011, 6 <sup>th</sup> Edition, Addison Wesley,	United States				
Ref	ference Books					
1.	Ernest O Doeblin, Measurement S	ystems, Appli	cation and	d design, 2013, 5 <sup>th</sup>		
	Edition McGraw Hill Book Co., Unite	ed States		-		
2.	Holman, J.P, Experimental methods	s for Engineer	s, McGra	w Hill Book Co., 2011, 8 <sup>th</sup>		
	Edition, United States	-				
3.	Robert Bosch Gmph, Automotive Hand Book, 2014, 9th Edition, Wiley, United States					
4	William, B. Ribbens, Understanding	Automotive E	lectronic	s, 2014, 8 <sup>th</sup> Edition Butter		
	Worth Heinemann, United States					
Мо	Mode of Evaluation: Continuous Assessment, Digital Assignment, Quiz and Final					
Ass	Assessment Test					
Re	Recommended by Board of Studies 28-07-2022					
App	Approved by Academic Council No. 67 Date 08-08-2022					

Course Code	Course Title			Т	Р	С
MEDS608L	Intelligent IOT System Design and Architecture			0	0	2
Pre-requisite	NIL Syllabu			s ve	ersio	on
		1.0				

The course is aimed at:

- 1. To explore the characteristics of the Internet of things and its design.
- 2. To enable the students to get familiar with IoT architecture models.
- 3. To acquaint the students with various security concepts and data analytics in the IoT system.
- 4. To develop and deploy an IoT enabled prototypes for real-life use cases.

#### **Course Outcome**

At the end of the course, the student will be able to

- 1. Assimilate the technologies that enable IoT and to interpret the different components in IoT architecture.
- 2. Comprehend the concepts of edge computing and edge enabled solutions for real-time industrial applications.
- 3. Envision the IoT communication architecture models and the protocol stack for the cost-effective design of IoT applications on different platforms.
- 4. Interpret the security threats and to design a resilient IoT Architecture.
- 5. Perceive the data analytics tools and gain knowledge to devise an intelligent IoT system.
- 6. Analyze cloud platform services to perform IoT data analytics and make the system intelligent.
- 7. Design and develop smart IoT prototypes for use cases under discussion.

#### Module:1 | IoT Essentials

4 hours

Evolution of IoT, IoT characteristics, IoT enabling technologies, Planning for an IoT solution, IoT use case development - Need and goals, IoT Architecture reference model, Functional blocks of IoT- Communication and security Model, Service oriented architecture, Event-driven architecture, Applications and standards.

# Module:2 | Edge Computing

hours

Introduction to Edge/Fog computing, Edge nodes and gateway, Node to edge interfaces, Protocol and standards for edge devices, IoT edge architecture, IoT supported hardware-Raspberry pi, ARM Cortex Processors, Software Platforms for IoT Edge - Raspbian Pi OS, RIOT, Python packages for edge computing, Edge security, Real time applications of edge computing.

# Module:3 IoT Communication Architecture and Protocols

5 hours

Communication models for IoT, 6LoWPAN, IPv4/IPv6, IoT communication protocols - MQTT, CoAP, LoRaWAN, RTLS, RPL, Communication API's.

### Module:4 | IoT Security and Privacy

4 hours

IoT risks and security challenges, IoT security architecture - A trust model, Restricting network access through security groups- Specific user access control, Data confidentiality and availability, User Authentication/Authorization methods, Block chain for IoT security and privacy.

#### Module:5 | Smart Data Analytics

4 hours

Need for data analytics, Data generation, Data pre-processing, Handling imbalanced data sets, Missing values, Outliers, Intelligent IoT systems –Supervised and Unsupervised machine learning algorithms, Deep learning for IoT- Predictive analytics, Python functions and modules for data analytics, Big Data analytics and frameworks

# Module:6 Data Analytics in Cloud Concepts

4 hours

Layered cloud architecture for data analytics, Elasticity in cloud for data warehousing,

Virtualization for Data-center automation, Real-time cloud data analytics tools, Al Services-Data based decisions, Cloud data lake, Exploratory data analysis, Open source cloud platforms and services. Module:7 | IoT Architecture for specific use cases 2 hours Roadmap for complete IoT solution, Open source IoT platforms, IoT solution to Health care, Automotive applications, Smart IoT architecture for Retail, Logistics and Farming, Intelligent IoT architecture for Home automation, Industry applications, Smart city and other applications to cater the societal requirements. Module:8 | Contemporary Issues 2 hours Total Lecture hours: 30 hours Text Book(s) ArshdeepBahga, Vijay Madisetti, "Internet of Things - A hands-on approach". Universities Press, 2015. John R. Vacca, "Cloud Computing Security: Foundations and Challenges", CRC Press, 2. Dey, Hassanien, Bhatt, Ashour and Satapathy "Internet of Things and Big Data Analytics towards Next-Generation Intelligence", Springer, 2018. Reference Books Adrian McEwen & Hakim Cassimally, "Designing the Internet of Things", Wiley, 2013. OvidiuVermesan, Peter Friess, "Internet of Things: Converging Technologies for Smart Environments and Integrated Ecosystems", River Publishers, 2013. Olivier Hersent, David Boswarthick, Omar Elloumi, "The Internet of Things - Key applications and Protocols", Wiley Publication, 2012 Mode of Evaluation: Continuous Assessment, Digital Assignment, Quiz and Final Assessment Test Recommended by Board of Studies 28-07-2022 Approved by Academic Council No. 67 Date 08-08-2022

Course Code	Course Title	L	Т	Р	С
MEDS608P Intelligent IOT System Design and Architecture Lab		0	0	2	1
Pre-requisite	NIL	Syllabus version			rsion
		1.0			

The course is aimed at:

- 1. To explore the characteristics of the Internet of things and its design.
- 2. To enable the students to get familiar with IoT architecture models.
- 3. To acquaint the students with various security concepts and data analytics in the IoT system.
- 4. To develop and deploy an IoT enabled prototypes for real-life use cases.

#### **Course Outcome**

At the end of the course, the student will be able to

- 1. Assimilate the technologies that enable IoT and to interpret the different components in IoT architecture.
- 2. Comprehend the concepts of edge computing and edge enabled solutions for real-time industrial applications.
- 3. Envision the IoT communication architecture models and the protocol stack for the cost-effective design of IoT applications on different platforms.
- 4. Interpret the security threats and to design a resilient IoT Architecture.
- 5. Perceive the data analytics tools and gain knowledge to devise an intelligent IoT system.
- 6. Analyze cloud platform services to perform IoT data analytics and make the system intelligent.

In	dicative Experiments				
1	Task-1				8 hours
	Program the gateways to interfac	e the sensors an	d implemen	t various IoT	
	communication protocols to perfo	rm secured edge	computing	<u>-</u>	
2	Task -2				8 hours
	Explore the open source IoT platf	orms to build dat	a driven inte	elligent	
	Industry 4.0 applications using vir	tual things.			
3 Task-3:				7hours	
	Build prototypes and explore UI/L	JX, data analytics	tools for		
	Internet of Medical Applications.				
4	Task-4:				7 hours
	Explore the open source cloud pla	atforms to perforn	n environme	ental	
	monitoring / smart agriculture / inf	ternet of vehicles	and other in	nnovative	
intelligent IoT use cases.					
			Total Labo	ratory Hours	30 hours
Mo	ode of Assessment: Continuous As	sessment and Fi	nal Assessr	nent Test	
Re	ecommended by Board of Studies	28-07-2022			
Ap	Approved by Academic Council No. 67 Date 08-08-2022				

Course Code	Course Title				Р	С
MEDS609L	Fault Tolerance and Dependable Systems				0	3
Pre-requisite	NIL	Syllabus version			ion	
		1.0				

The course is aimed at:

- 1. Providing students with a working knowledge of the potential faults and errors occurring in an embedded system.
- 2. Providing knowledge in concepts of fault detection and fault tolerance.
- 3. Teaching students dependability concepts
- 4. Exposing the fault tolerance strategies and design techniques.

#### **Course Outcome**

At the end of the course, the student will be able to

- 1. Gain knowledge in concepts involving fault detection
- 2. Comprehend dependability concepts
- 3. Understand tolerance and correction mechanisms in real world scenarios.
- 4. Design and develop dependable systems for mission critical applications.
- 5. Understand Fault tolerance in interconnected systems.
- 6. Understand Fault tolerance in distributed systems.
- 7. Apply Dependability evaluation techniques and Tools

Module:1	Faults and Failures	4 hours						
Fault - erro	or, failure - faults and their manifestation - classifi	cation of faults and failures						
Module:2	Dependability Concepts	5 hours						
Dependab	e system - techniques for achieving dependabilit	y - dependability measures						
Module:3	Fault Tolerance Strategies	6 hours						
Fault detec	ction – masking – containment – location – recon	figuration - recovery						
Module:4	Fault tolerant design techniques	8 hours						
Hardware	Hardware redundancy - software redundancy - time redundancy - information redundancy							
Module:5	Fault tolerance in Interconnects	6 hours						
Hypercube	- star graphs - fault tolerant ATM switches							
Module:6	Fault Tolerance in Distributed Systems	8 hours						
	General problem - consensus protocols - chec							
storage an	d RAID architectures - data replication and resilie							
Module:7	Dependability evaluation techniques and tools	6 hours						
Fault trees	- Markov chains - HIMAP tool							
Module:8	Contemporary Issues	2 hours						
	Total Lecture hours:	45 hours						
	Total Lecture nours:	45 nours						
Text Book	i(s)							
1. Israel	Koren, C. Mani Krishna, Fault-Tolerant System	s, 2011, Morgan Kaufmann, San						
Franci	SCO.							
	Dubrova, Fault-Tolerant Design, 2013, Springer,	Sweden.						
Reference	Books							

1.	D. P. Siewiorek and R. S. Swarz, Reliable Computer Systems: Design and Evaluation,						
	2014,3rded., Digital Press, Pennsylvania.						
2.	2. Alessandro Birolini, Reliability Engineering: Theory and Practice, 2017, 8th ed., Springer-						
	Verlag Berlin Heidelberg, Spain.						
Mode of Evaluation: Continuous Assessment, Digital Assignment, Quiz and Final							
Assessment Test							
Re	commended by Board of Studies	28-07-2022					
Approved by Academic Council		No. 67	Date	08-08-2022			

Course Code	Course Title				Р	С
MEDS611L	Parallel Processing and Computing			0	0	3
Pre-requisite	NIL	Syllabus version			on	
		1.0				

The course is aimed at

- 1. Teaching the students to understand the scope, design and model of parallelism and to know the parallel computing architecture
- 2. Teaching students to do analytical modelling and performance of parallel programs
- 3. Teaching students to solve a complex problem with message passing model
- 4. Programming with CUDA and analyse complex problems with shared memory programming

#### **Course Outcome**

At the end of the course the student will be able to

- 1. Understand the fundamentals of parallel processing
- 2. Illustrate the scheduling loops and process execution
- 3. Realize the parallel system architecture with CUDA
- 4. Comprehend the kernel based parallel programming concepts
- 5. Apply the performance consideration for parallel processing
- 6. Analyse various parallel computation patterns
- 7. Perform spare matrix vector multiplications

Module:1	Introduction to Parallel Processing	5 hours				
Parallel pr	ocessing – Concepts and Terminology- Parallel	Computer Memory Architectures -				
	ogramming Models - Designing Parallel Program	s- Performance Analysis				
Module:2	Shared Memory Programming	6 hours				
Processes	and Threads - Scope of Variables - Reduction	Clause – Directives – Scheduling				
Loops – Ca	Loops – Caches, Cache coherence and False Sharing – Thread Safety – Examples: Bubble-					
sort, Odd-	even transposition sort					
Module:3	Parallel Computing	6 hours				
Portability	and Scalability- Introduction to CUDA, Data F	Parallelism and Threads-Memory				
Allocation a	and Data Movement API- Kernel-Based SPMD Pa	arallel Programming-Kernel based				
Parallel Pr	ogramming, Multidimensional Kernel Configura	ation- Basic Matrix-Matrix				
Multiplicati	on					
Module:4	Kernel-Based Parallel Programming	6 hours				
	heduling-Control Divergence- Memory Model and					
	gorithms- Tiled Matrix Multiplication- Tiled Mati					
	Conditions in Tiling A Tiled Kernel for Arbitrary I					
Module:5	Performance Considerations	6 hours				
Warps and	d Thread execution - Global Memory Bandwidt	h - DRAM Bandwidth - Memory				
Coalescing	-Dynamic partition of execution resources					
	Introduction to Packaging &PCB Design	8 hours				
Convolutio	n- Tiled Convolution- 2D Tiled Convolution	Kernel- Data Reuse in Tiled				
Convolutio	n-Reduction- A Basic Reduction Kernel- Scan	(Prefix Sum) - A Work-Inefficient				
Scan Kern	el- A Work-Efficient Parallel Scan Kernel					
Module:7	High Speed PCB design and Analysis	6 hours				
	Wireless Standards					
Parallel Sp	oMV Using CSR-Padding and Transposition-U	sing Hybrid to Control Padding-				
	d Partitioning for Regularization	-				
Module:8	Contemporary Issues	2 hours				

		Tot	al Lecture ho	ours:	45 hours		
Te	xt Book	(s)					
1.	Ananta	Grama, Anshul Gupta, Geor	ge Karypis, V	ipin Kuma	ar, Introduction to		
	Parallel Computing, 2011, Second Edition, Addison Wesley Professional,						
	UK.	UK.					
2.	2. David B. Kirk and Wen-mei W. Hwu, Programming Massively Parallel Processors: A						
	Hands	-on Approach, 2016, Third Ed	dition, Morgan	<b>Kaufmar</b>	nn Publishers, US.		
Re	ference	Books					
1.	Pache	co, Peter. An Introduction to	Parallel progra	amming, 2	2011, First Edition, Morgan		
	Kaufm	ann Publishers, USA					
Мо	de of Ev	valuation: Continuous Assess	ment, Digital	Assignme	ent, Quiz and Final		
Ass	sessmer	nt Test		· ·			
Re	commer	nded by Board of Studies	28-07-2022				
Ap	pproved by Academic Council No. 67 Date 08-08-2022						

Course Code	Course Title		T	Р	С
MEDS613L	Cloud Computing		0	0	3
Pre-requisite	NIL	Syllabus version			on
		1.0			

The course is aimed at making the students to

- 1. To explore the cloud computing concepts.
- 2. To get familiar with cloud orchestration to support elasticity and edge device availability.
- 3. To impart knowledge on cloud security and to develop large scale embedded applications.

#### **Course Outcomes**

At the end of the course, the students will be able to

- 1. Comprehend the basics of cloud computing, cloud models and its connectivity to develop smart applications.
- Envision the virtualization techniques and Interpret a suitable cloud model to capture the business needs by interpreting different service delivery and deployment models.
- 3. Perceive the division of responsibility and managing risks in the cloud environment.
- 4. Analyse the system level security threats and to design a resilient cloud Architecture.
- 5. Assimilate the OS security concepts and ability to design a resilient cloud architecture.
- 6. Design and develop platform-specific tools and management consoles to build real-time embedded system applications.

# Module:1 Cloud Computing Fundamentals 6 hours Characteristics of Cloud computing – Cloud Architecture– Design considerations-

Characteristics of Cloud computing – Cloud Architecture– Design considerations-Edge device discovery, Cloud orchestration, Cloud connectivity for edge devices, Cloud Models – Cloud Services – IaaS, PaaS, SaaS, XaaS.

#### Module:2 | Cloud Technologies

6 hours

Virtualization, Load Balancing and fault tolerance, Scalability, Elasticity, Deployment, Replication, Monitoring, Software defined Networking, Network function Virtualization, Mapreduce programming model.

# Module:3 Cloud Computing Services

6 hours

Compute Services, Storage Services, Database services, Application Services, Data Analytics Services for predictive maintenance, Deployment and Management Services, Identity and Access management services.

#### Module:4 | Cloud Risk Analysis

6 hours

Managing Risks in the Cloud. Retaining Information Security Accountability. Managing User Authentication and Authorization. Negotiating Security Requirements with Vendors, Service Level Agreement.

#### Module:5 | Secure Cloud Architecture

6 hours

Restricting Network Access through Security Groups. Specific User Access Control, Integrating Cloud Authentication/Authorization, Data Confidentiality and Availability, Securing Data in Motion and Data at Rest, Identifying Your Security Perimeter, Key Management.

6 hours

# Module:6 OS Security Program threats, System threats, Locking Down

Program threats, System threats, Locking Down Cloud Servers. Patching Vulnerabilities, Filtering Traffic by Port Number, Operating System Security Policies and Procedures.

# Module:7 Cloud Platforms 7 hours

Google cloud, Microsoft Azure, Amazon Web services, Cloud application development using third party APIs, Resource pooling, Cloud service migration, Federated cloud platform, Embedded systems applications on cloud.

Module:8 | Contemporary Issues | 2 hours

Total Lecture hours: 45 hours

#### Text Book(s)

- 1. Cloud Computing theory and Practice, 3rd Edition by Dan Marinescu, Elsevier, 2021.
- Cloud computing: Methodology, Systems and Applications, Lizhe Wang, Rajiv Ranjan, Jinjun Chen, CRC Press, 2017.
- 3. Cloud Computing Principles and Paradigms, Rajkumar Buyya, James Broberg, Andrzej Goscinski, John Wiley & Sons, Inc. 2011.

#### Reference Books

- John R. Vacca, "Cloud Computing Security: Foundations and Challenges", CRC Press, 2016.
- Pearson, Siani, Yee, George, "Privacy and Security for Cloud Computing", Springer, 2013.
- 3. Nick Antonopoulos, Lee Gillam, Cloud Computing: Principles, Systems and Applications, Springer, 2015.
- 4. Toby Velte, Anthony Velte, Robert Elsenpeter, Cloud Computing, A Practical Approach, McGraw Hill, 2010.

Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test

Recommended by Board of Studies 07-06-2023		023	
Approved by Academic Council	No. 70	Date	24-06-2023

Course Code	Course Title	L	T	Р	С
MEDS614L	Cyber Physical Systems	3	0	0	3
Pre-requisite	NIL	Syllabus version			on
		1.0			

The course is aimed at:

- 1. To introduce the fundamentals of modelling cyber-physical systems (CPS) consisting of both discrete and continuous dynamics
- 2. To provide an overview of design automation and verification problems with a systems perspective for designing, monitoring, and managing large scale infrastructure
- 3. To provide exposure to practical applications of modelling and verification through case studies and able to address real-world problems through Cyber Physical Systems.

#### Course Outcomes

At the end of the course, the student will be able to

- 1. Understand the need and purpose of the different components of Cyber Physical Systems.
- 2. Ideate, design, and prototype
- 3. Design their own system with different applications
- 4. Build systems with mathematical modelling in various fields with parametric measures
- 5. Evaluate the performance of a Cyber Physical System
- 6. Have hands on experience in using state-of- art hardware and software tools by synthesis and learning for cyber-physical system design and adaptation
- 7. Verify safety, privacy, and security for the designed cyber physical systems
- 8. Deploy cyber physical systems in practical applications like Internet of things (IoT), swarm systems, edge computing, and smart gateways.

# Module:1 Cyber Physical Systems

5 hours

Motivation, overview, requirements, features and examples of Cyber-Physical Systems (CPS) in the real world; Key design drivers and quality attributes of CPS. Attributes of high confidence CPS, Interface between Physical and Cyber World: Industry 4.0, AutoSAR, IIOT implications, Building Automation, Medical CPS, Transportation, Energy, etc.

#### Module:2 CPS - Modelling Dynamic Behavior

7 hours

Basic principles of design and validation of CPS, Relationship between embedded systems and CPS, Design Process- Modeling, Design, Analysis, Continuous Dynamics - Discrete Dynamics. Hybrid Systems - State Machines - Concurrent Models of Computation

#### Module:3 CPS- Design and Implementation

7 hours

Real-Time Operating Systems. Networking Embedded Systems. Sensors and Actuators. Embedded Processors - Memory Architecture - Input and Output. Multitasking – Scheduling, CPS case study- design, implementation

# Module:4 CPS- Analysis and Verification

5 hours

Invariants and Temporal Logic - Equivalence and Refinement. Evaluate the performance. Reachability analysis - Quantitative analysis. CPS Case Study-Analysis, Verification, etc.

7 hours

#### Module:5 CPS- Network and Protocol

CPS Communications, CPS Network – Wireless Hart, CAN, Automotive Ethernet, Scheduling Real Time CPS tasks, data analysis, and visualization. Secure Hardware, CPS Models and Aspects, Internet of Things Architectures, Properties, and Security Requirements; CPS vs IoT; Network and Protocol Case Studies; Constrained Application Protocol: Application Layer Connection-Less Lightweight Protocol for the Internet of Things; Datagram Transport Layer Security. Overview and Supporting Constrained Application Protocol.

# Module:6 | ČPS- Security Issues and Controls

6 hours

Security Challenges – Quantifying Security & Risk – Trustworthy Operational Readiness –Security Technologies. CPS Security Vulnerabilities, Real-World CPS Attacks, Security Control and Solutions. Securing Case Studies- the Future Autonomous Vehicle, Networking Technologies, Wireless Sensor Networks, Transportation, IPv6-Connected Internet of Things, Machine-to-Machine Communications, Mobile Cloud Computing.

# Module:7 Machine Learning for Cyber Physical Systems

6 hours

Introduction to Machine Learning. Mathematical Optimization - Planning and guidance. Basics of Neural Networks. Deep Learning. Supervised Learning, Unsupervised Learning, Ensemble Learning, Machine Learning for Cyber Physical Systems: Vehicular CPS, Smart Cities and the Internet of Everything, Drones as CPS.

Module:8	Contemporary Issues		2 hours
		Total Lecture hours:	45 hours

#### Text Book(s)

- 1. E.A.Lee and S A Shesia, (2018), Embedded system Design: A Cyber-Physical Approach, Second Edition, MIT Press.
- 2. Ragunathan (Raj) Rajkumar, Dionisio de Niz and Mark Klein, (2017), Cyber Physical Systems, Pearson Education; First edition, ISBN-10: 9386873567
- B. Rajeev Alur, "Principles of Cyber-Physical Systems", MIT Press, 2015.

#### Reference Books

- 1. Houbing Song, Danda B Rawat, Sabina Jeschke, and Christian Brecher, "Cyber-Physical Systems: Foundations, Principles and Applications (Intelligent Data-Centric Systems: Sensor Collected Intelligence)", Academic Press, 2016.
- 2. Peter Marwedel, "Embedded System Design-Embedded Systems Foundations of Cyber-Physical Systems", 2nd edition, SIE, 2013.
- 3. André Platzer. Foundations of Cyber-Physical Systems. Lecture Notes, Computer Science Department, Carnegie Mellon University. 2013.
- 4. Alexander Romanovsky, Fuyuki Ishikawa (eds,) Trustworthy Cyber-Physical Systems Engineering-Chapman and Hall CRC (2016).

Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test

Recommended by Board of Studies	07-06-20	)23	
Approved by Academic Council	No. 70	Date	24-06-2023

Course Code	Course Title	L	Т	Р	С
MEDS614P	Cyber Physical Systems Lab	0	0	2	1
Pre-requisite	NIL	Sylla	abus v	/ersio	n
			1.0	)	

The course is aimed at:

- 1. To introduce the fundamentals of modeling cyber-physical systems (CPS) consisting of both discrete and continuous dynamics
- 2. To provide an overview of design automation and verification problems with a "systems" perspective for designing, monitoring, and managing large scale infrastructure
- 3. To provide exposure to practical applications of modeling and verification through case studies and able to address real-world problems through Cyber Physical Systems.

#### **Course Outcomes**

At the end of the course, the student will be able to

- 1. Ideate, design, and prototype
- 2. Design their own system with different applications
- 3. Build systems with mathematical modeling in various fields with parametric measures
- 4. Have hands on experience in using state-of- art hardware and software tools.
- 5. Understand automotive electronics architecture (sensors, actuators, computing, connectivity, control) design.
- 6. Understand highly dynamic networked systems (lifetime management, connectivity, adaptation).
- 7. Understand Security/safety for automotive systems.
- 8. Understand Integration of learning and optimization into safety-critical systems.

ln	dicative Experiments	
1	Task-1: Embedded C/C++ Programming for CPS	7 hours
	Sub task 1: Port Handling, Timer initialization	
	Sub task 2: Waveform Generation.	
	Sub task 3: Serial Port Controller	
	Sub task 4: Interrupt Generation	
	Sub task 5: Motor Control using Embedded C	
	Sub task 6: PLC Emulation using Embedded C	
	Sub task 7: Pulse Width Modulation	
2	Task-2: Benchmark IoT for CPS	6 hours
	Sub task 1: Deployment of Sensors and IoT devices	
	Sub task 2: Control of sensors using Open APIs like MQTT,	
	COAP	
	Sub task 3: Addition of new sensors to CPS-IoT.	
	Sub task 4: Control of Servo Motors using Embedded Software	
3	Task-3: Modeling and Simulation of CPS using Ptolemy	9 hours
	Sub task 1: Computation Models	
	Sub task 2: Process Networks	

	Sub task 3: Discrete Events Sub task 4: Data Flow				
	Sub task 5: Rendezvous Based models				
	Sub task 6: Synchronous/Reactive				
	Sub task 7: 3D Visualization				
	Sub task 8: Continuous Time Model				
	Sub task 9: Hybrid Systems Modeling				
	Sub task 10: Sensor Network Design				
	Sub task 11: Scientific workflows				
	Sub task 12: Modeling and Simulation of Wireless Networks				
4	Task-4: Matlab toolboxes	8 hours			
	Sub task 1: Simulink, Stateflow, Define embedded systems and				
	cyber-physical systems (CPS) and give examples Sub task 2: Understand various modeling formalisms for CPS,				
	such as hybrid automata, state-space methods, etc.				
	Sub task 3: Understand CPS design, modeling, and analysis				
	Compare architectural design trade-offs in CPS				
	Sub task 4: Design CPS and analyze models of CPS to see if				
	they meet their specifications and requirements Sub task 5: Understand methods for verification and validation				
	of CPS such as simulation, testing, model checking, etc.				
	Sub task 6: Understand and appreciate engineering design and				
	analysis difficulties in CPS disciplines				
5	Additional Exercises  Matlab and Simulink				
	Robotic Control and Simulation				
	Drone Control				
	Automotive Systems				
	Total Laboratory Hours 30 hours				
M	ode of Assessment: Continuous Assessment and Final Assessment To	est			
	ecommended by Board of Studies 07-06-2023  oproved by Academic Council No.70 Date 24-06-2023				
	24-00-2023				

Course Code	Course Title	L	T	Р	С
MEDS615L	5G and Future Generation Communication Systems	3	0	0	3
Pre-requisite	NIL	Sylla	bus	vers	ion
		1.0			

The course is aimed at making the students to

- 1. To understand standardization and the evolution of neXt Generation networks.
- 2. To explore the new terminologies and concepts relating to NR.
- 3. To provide exposure to different 5G use cases and practical applications.

#### **Course Outcomes**

At the end of the course, the students will be able to

- 1. Understand the 3GPP 5G standards and spectrum.
- 2. Comprehend the key concepts, terminologies and access methods of 5G NR.
- 3. Envisage the 5G Random Interface Architecture.
- 4. Analyze the MIMO techniques for 5G NR.
- 5. Evaluate different 5G use cases and applications.
- 6. Explore the future Generation and private networks relating to applications.

#### Module:1 | 5G - Introduction

4 hours

Evolution of Wireless Technologies (1G to 4G), What is 5G? Why do we need 5G? 5G Standardization - 3GPP and IMT2020 - Spectrum for 5G, 5G deployment - Options, Challenges.

# Module:2 | 5G NR – Terminologies and Concepts

7 hours

5G Network Terminology and concepts - Channel Access methods - Comparison, Massive centralised RAN, Cognitive Radio, Vehicular communication, Network slicing.

#### Module: 3 | 5G NR Radio Interface architecture

8 hours

Overall system architecture - Radio Protocol Architecture, QoS handling, User Plane Protocols-Radio Link Control - Medium-Access Control – Physical Layer functions - Control Plane Protocols, Mobility.

# Module:4 Advance Multiple access and MIMO techniques

Overview of Multi-Antenna Techniques in LTE, Moving to 5G Cellular with Large-scale Antenna Arrays, Antenna-array Architectures for 5G Cellular, Massive MIMO for Evolved LTE Systems (Below 6 GHz), Massive MIMO for cmWave and mmWave Systems (Above 6 GHz), Advanced Multiple-access and MIMO Techniques - NOMA.

# Module:5 | 5G NR use-cases and applications

4 hours

5G NR Service Classes Overview: Enhanced Mobile Broadband (eMBB), Massive Machine-Type Communications (m-MTC), Ultra Reliable Low Latency Communications (URLLC), Application of NFV and SDN to 5G Infrastructure.

#### Module:6 | M2M Communications

8 hours

LTE evolution for M2M, 5G for M2M communication, Low-latency Radio-interface Perspectives for Small-cell 5G Networks - New Radio-interface Design for Low-latency 5G Wireless Access, Massive Internet of Things.

#### Module:7 | Future Generation networks

4 hours

NR beyond 52.6 GHz, IAB enhancements, NR – Broadcast / Multicast, General enhancements, Towards 6G.

Mo	dule:8	Cc	ntem	porar	y Issu	ies				2 hours
Indu	ustry ex	pert	lectu	ire on	differe	nt 5G	use case	S		
							Total	Lecture h	ours:	45 hours
Tex	t Book	(s)								
1.	Erik D	Dahl	man,	Stefa	n Park	wall, .	Johan Sk	old "5G N	R: The	Next Generation
	Wirele	ess A	Acces	s Tec	hnolog	y", Ac	ademic P	ress, 1st E	dition,	2018.
2.	R. Var	nnith	namby	y and	S. Talv	var, "⊺	Fowards 5	G: Applica	itions, F	Requirements and
								ons, 1st Ed		
3.	Saad	Z. <i>P</i>	sif, "S	5G Mc	bile C	ommı	ınications	Concepts	and Te	echnologies, CRC
	Press,									
4.					"Funda	ament	als 5G Mo	bile Netwo	rks", Jo	ohn Wiley & Sons,
	1 <sup>st</sup> Edi	ition	, 201	5.						
Ref	erence	e Bo	oks							
1.	Robe	rt W	. Hea	th Jr.,	Angel	Loza	no, "Foun	dations of	MIMO	Communication",
							Edition, 2			
2.								ng, "Mass		
	Networks: Selected Applications", Springer, 1st Edition, 2018									
					tinuous	s Ass	essment	Fest, Digita	al Assi	gnment, Quiz and
	al Asses									
	commer					lies	07-06-20	)23		
App	proved b	эу А	cader	nic Co	uncil		No. 70	Date	24-06	6-2023

Course Code	Course Title	L	T	Р	С
MEDS616L	Machine Leaning and Deep Learning	3	0	0	3
Pre-requisite	NIL	Sylla	bus	versi	on
			1.0	)	

The course is aimed at

- Understanding about the fundamentals of machine learning and neural networks
- 2. Enabling the students to acquire knowledge about pattern recognition.
- 3. Motivating the students to apply deep learning algorithms for solving real life problems.

#### **Course Outcomes**

At the end of the course the student will be able to

- 1. Comprehend the categorization of machine learning algorithms.
- 2. Understand the types of neural network architectures, activation functions
- 3. Acquaint with the pattern association using neural networks
- 4. Explore various terminologies related with pattern recognition
- 5. Adopt different feature selection and classification techniques
- 6. Understand the architectures of convolutional neural networks and Comprehend advanced neural network architectures such as RNN, Autoencoders, and GANs.

# Module:1Learning Problems and Algorithms4 hoursVarious paradigms of learning Unsupervised algorithmsproblems, Supervised, Semi-supervised and Semi-supervised and Semi-supervised and Semi-supervised8 hours

Differences between Biological and Artificial Neural Networks - Typical Architecture, Common Activation Functions, Multi-layer neural network, Linear Separability, Hebb Net, Perceptron, Adaline, Standard Back propagation

# Module:3 Neural Network – II 8 hours

Training Algorithms for Pattern Association - Hebb rule and Delta rule, Hetero associative, Auto associative, Kohonen Self Organising Maps, Examples of Feature Maps, Learning Vector Quantization, Gradient descent, Boltzmann Machine Learning

# Module:4 Machine Learning: Terminologies 7 hours

Classifying Samples: The confusion matrix, Accuracy, Precision, Recall, F1- Score, the curse of dimensionality, training, testing, validation, cross validation, overfitting, under-fitting the data, early stopping, regularization, bias and variance

# Module:5 Machine Learning: Feature Selection and Classification 7 hours

Feature Selection, normalization, dimensionality reduction, Classifiers: KNN, SVM, Decision trees, Naïve Bayes, Binary classification, multi class classification, clustering.

# Module:6 | Convolutional Neural Networks 5 hours

Feed forward networks, Activation functions, backpropagation in CNN, optimizers, batch normalization, convolution layers, pooling layers, fully connected layers, dropout, Examples of CNNs.

Мо	dule:7	RNNs, Auto encoders an	d GANs			4 hours
Sta	ate, Stru	cture of RNN Cell, LSTM an	d GRU, T	ime distr	ibuted lay	ers, Generating
		encoders: Convolutional A				
		auto encoders, GANs: The	discrimina	tor, gene	erator, DC	GANs
		Contemporary Issues				2 hours
Gu	est Lect	ures from Industry and, Rese	earch and	Develop	ment Org	anizations
			Total	Lecture	hours:	45 hours
Tex	t Book	(s)				
1.	J. S. R	. Jang, C. T. Sun, E. Mizu	tani, Neu	ro Fuzz	y and Sc	oft Computing -
	A Com	putational Approach to L	earning a	ind Mad	hine Inte	elligence, 2012,
	PHI le	arning	_			_
2.		Learning, Ian Good fellow,		Bengio a	and Aaror	n Courville, MIT
	Press,	ISBN: 9780262035613, 201	16.			
Ref	ference	Books				
1.		lements of Statistical Lear		vor Hast	tie, Robe	rt Tibshirani and
	Jerom	e Friedman. Second Edition	. 2009.			
2.	Unders	standing Machine Learning	ShaiSha	lev-Shw	artz and	Shai Ben-David.
	Cambr	idge University Press. 2017				
Мо	Mode of Evaluation: Continuous Assessment, Digital Assignment, Quiz and Final					
Ass	Assessment Test					
Red	commer	nded by Board of Studies	07-06-20	)23		
App	oroved b	y Academic Council	No. 70	Date	24-06-20	)23

Course Code	Course Title	L	Т	Р	С
MVLD611L	Advanced Computer Architecture	3	0	0	3
Pre-requisite	NIL	Sylla	bus v	versi	on
			1.0		

The course is aimed to

- 1. Introduce advanced concepts of computer architecture.
- 2. Acquire knowledge on various interconnect topology for multiprocessor system and Different pipelining techniques.
- Understanding different memory hierarchy for multiprocessor and multicomputer systems.

#### **Course Outcomes**

At the end of the course the student will be able to:

- Understand the architecture of the various multiprocessors and multicomputer.
- 2. Determine the required static or dynamic interconnect network for a multiprocessor system.
- 3. Understand the Data level parallelism in Vector architecture, SIMD, GPU
- 4. Apply different pipelining techniques to reduce computation time.
- 5. Analyse the various memory design for multiprocessor and multicomputer.
- 6. Design scalable parallel architecture for multiprocessor system.

# Module:1 | Parallel computer models

5 hours

The state of computing - Conditions of parallelism - Data and resource Dependences - Hardware and software parallelism - Program partitioning and scheduling - Grain Size and latency Classification of parallel computers - Multiprocessors and Multicomputer

# Module:2 | System Interconnect Architectures

7 hours

Network properties and routing - Static interconnection Networks - Dynamic interconnection Networks - Multiprocessor system Interconnects - Hierarchical bus systems - Crossbar switch and multiport memory - Multistage and combining network.

#### Module:3 Data level Parallelism in Vector and GPU Architectures 7 hours

Vector computation instructions,

Registers and dynamic typing, loads and store, parallelism during vector execution, SIMD Instruction extension for multimedia-Graphics Processing Units- Detecting and enhancing loop-level parallelism

# Module:4 Pipelining

7 hours

Linear pipeline processor - nonlinear pipeline processor - Instruction pipeline Design - Mechanisms for instruction pipelining - Dynamic instruction scheduling - Branch Handling techniques - branch prediction - Arithmetic Pipeline Design.

#### Module:5 | Memory Hierarchy Design

6 hours

Cache basics & cache performance - reducing miss rate and miss penalty - multilevel cache hierarchies - main memory organizations - design of memory hierarchies.

#### Module:6 | Shared Memory Architectures

6 hours

Symmetric shared memory architectures – distributed shared memory architectures cache coherence protocols – scalable cache coherence – directory protocols – memory-based directory protocols – cache-based directory protocols. Module:7 | Multiprocessor Architectures 5 hours Computational models - An Argument for parallel Architectures - Scalability of Parallel Architectures – Benchmark Performances. Module:8 | Contemporary Issues 2 hours Guest lectures from Industries and R & D Organizations Total Lecture hours: 45 hours Text Book(s) Kai Hwang, NareshJotwani, Advanced Computer Architecture: Parallelism, Scalability, Programmability, 2017, Third edition, Tata McGraw Hill Education, India. David Patterson, Andrew Waterman, The RISC-V Reader: An Open Architecture Atlas, 2017, First edition, Strawberry Canyon, USA. Reference Books John L. Hennessy, David A. Patterson, Computer Architecture: A Quantitative Approach, 2011, Fifth edition, Morgan Kaufmann. DezsoSima, Terence Fountain, Peterr Karsuk, Advanced computer 2. Architectures – A Design Space Approach, 2014, Pearson Education, India. Ananth Grama, Anshul Gupta, George Karypis and Vipin Kumar, -Introduction to Parallel Computing, 2009, Second edition, Pearson Education, India. Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test. Recommended by Board of Studies 07-06-2023 Approved by Academic Council No. 70 Date 24-06-2023

ourse Title L T P	С
Design with FPGA 3 0 0	3
Syllabus ver	sion
1.0	
	Course Title L T P  1 Design with FPGA 3 0 0  Syllabus ver  1.0

This course is aimed to

Provide an overview of FPGA architectures and expound on the softcore and hard- core processors in association with hardware and software co-design.

- 2. Understand the specification and operation of Programming for peripheral Interfaces and Interconnect Fabrics.
- 3. Implement digital system and IP blocks for various DSP algorithms.

# Course Outcomes:

After completion of the course the student will be able to:

- 1. Understand and get an idea about SoC and FPGA architectures.
- 2. Understand the NIOS II soft core processor architecture.
- 3. Analyze the working of hardware and software co-design flow.
- 4. Interpret the usage of various peripheral interfaces for system design.
- 5. Develop a system by choosing suitable interconnect fabrics.
- 6. Design the system using NIOS II soft core processor, model the system by using IP block and design and develop embedded synthesis using FPGA.

Module:1 SoC Architecture	6 hours
An Overview of System on Design – FPGA SoC Architecture – Case S	tudy: Xilinx
/ Intel FPGA	
Module:2 Soft Core and Hard Core Processor	10 hours
Processor Architecture and Configurability Features: Nios II Processor –	Nios
V Processor – ARM cortex A9 architecture	
Module:3   Hardware - Software Co-design Flow	2 hours
Hardware Design Flow - Software Design Flow - EDA Tool Hardware an	d
Software design flow	
Module:4 Programming for peripheral Interfaces	5 hours
LCD, PS2, RS232, SDRAM, SRAM Controller, VGA, Audio and Video, I	PIO,
External Bus bridge, and IrDA	
Module:5 Interconnect Fabrics	4 hours
Avalon Switch Fabric Interconnect - Implementation and Function	is-Integrated
Design Environment	
Module:6 System Design	8 hours
Traffic light Controller, Real Time Clock - Interfacing using FPGA: VGA, Lo	
Module:7 IP cores based SoC design	8 hours
Edge detection algorithm- Image edge detection in FPGA using SOBEL	
Detection/ Canny Edge Detection Algorithm, Colour and Brightness Enh	
algorithm- Contrast enhancement using RGB to HSV algorithm based o	n FPGA –
SRAM Configuration using Controllers	
Module:8 Contemporary Issues	2 hours
Guest lecture from Industry and R & D Organizations	
Total Lecture hours:	45 hours
Text Book(s)	

	ZainalabedinNavabi, "Embedded Core Design with FPGAs", 2011, Tata					
	MCGraw Hill Ltd, India.					
2.	Pong P. Chu, Embedded SoPC Design with NIOS II Processor and VERILOG examples", 2012, Wiley, USA.					
۷.	VERILOG examples", 2012, Wiley, USA.					
Reference Books						
1	Donald G. Bailey," Design for Embedded Image Processing on FPGAs", 2012, Wiley, USA.					
2	Jivan S. Parab, Rajendra S Gad, G.M. Naik, "Hands-on Experience with Altera FPGA Development Boards", 2018, Springer, USA.					
3	Joseph Yu, System-on-Chip Design with Arm Cortex-M Processors, 2019, ARM Education Media					
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and						
Final Assessment Test.						
Recommended by Board of Studies 07-06-2023						
Approved by Academic Council No. 70 Date 24-06-2023						
	<u> </u>					

Course Code	Course Code Course Title		T	Р	С
MVLD616L	Scripting Languages For Electronic Design Automation	3	0	0	3
Pre-requisite	NIL	Syll	abus	versi	on
		1.0			

The course is aimed to

- To write scripts in the LINUX environment.
- 2. To study the principles of Scripting Languages like Perl, TCL and Python.
- 3. To write the scripts for automation using the languages like Perl, TCL and Python.

#### Course Outcomes:

At the end of the course the student will be able to

- 1. Explain and apply commands in LINUX environment.
- 2. Develop and execute the Perl scripts.
- 3. Analyze and Handle files, directories and manage processes using Perl scripts.
- 4. Use TCL scripts for automation.
- 5. Build TCL scripts to Handle files, directories and manage process.
- 6. Develop Python scripts to interpret files and directories.

#### Module:1 LINUX Basics 5 hours Introduction to Linux, File System of Linux, General usage of Linux Kernel and Basic Commands, Linux users and group, Permissions for file, directory and users, Searching a file and directory, zipping and unzipping concepts. Module:2 PERL Basics 7 hours History and Concepts of PERL - Scalar Data - Arrays and List Data - Control structures - Hashes - Basics I/O - Regular Expressions - Functions - Miscellaneous control structures - Formats. Module: 3 | Advanced Topics in PERL 6 hours Directory access - File and Directory manipulation - Process Management -Packages and Modules -Applications of PERL scripts to Electronic Design Automation. Module:4 | TCL Basics 7 hours An Overview of TCL and Tk -Tcl Language syntax – Variables – Expressions – Lists - Control flow - procedures - Errors and exceptions - String manipulations Module:5 | Advanced Topics in TCL 6 hours Accessing files - Processes. Applications - Controlling Tools - Basics of Tk. Module:6 Python Basics 6 hours Introduction to Python – Using Python interpreter – Brief tour on standard library -Control flow Tools – Data structures – Regular Expressions. Module:7 Advanced Topics in Python 6 hours Input and Output - Errors and Exceptions - Classes - Modules- Applications of Python scripts to Electronic Design Automation. Module:8 Contemporary Issues: 2 hours Guest lectures from Industry and R&D Organizations

Total Lecture hours:

45 hours

Text Book(s)							
1.	Larry Wall, Tom Christiansen, John Orwant, Programming PERL, 2012,						
	Fourth Edition, Oreilly Publications.						
2.	John K. Ousterhout, Ken Jones, Tcl and the Tk Toolkit, 2010, Second Edition,						
	Pearson Education, India						
Reference Books							
1.	Guido van Rossum Fred L. Drake, Jr., editor, Python Tutorial Release 3.2.3,						
	2012, Python Software Foundation.						
2.	Randal L. Schwartz, Brian D Foy, Tom Phoenix, Learning Perl, 2021, 8th						
	Edition, O'Reilly Media, Inc.						
3.	Mark Lutz, Learning Python, 2013, 5th Edition, O'Reilly Media, Inc.						
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and							
Final Assessment Test							
Red	commended by Board of Studies	07-06-2023					
App	proved by Academic Council	No. 70	Date	24-06-2023			