VIT®

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

SCHOOL OF ELECTRONICS ENGINEERING

M. Tech VLSI Design

(M.Tech MVD)

Curriculum

(2023-24 Admitted Students)

VISION STATEMENT OF VELLORE INSTITUTE OF TECHNOLOGY

Transforming life through excellence in education and research.

MISSION STATEMENT OF VELLORE INSTITUTE OFTECHNOLOGY

World class Education: Excellence in education, grounded in ethics andcritical thinking, for improvement of life.

Cutting edge Research: An innovation ecosystem to extend knowledge andsolve critical problems.

Impactful People: Happy, accountable, caring and effective workforce and students.

Rewarding Co-creations: Active collaboration with national & international industries & universities for productivity and economic development.

Service to Society: Service to the region and world through knowledge and compassion.

VISION STATEMENT OF THE SCHOOL OF ELECTRONICSENGINEERING

To be a leader by imparting in-depth knowledge in Electronics Engineering, nurturing engineers, technologists and researchers of highest competence, who would engage in sustainable development to cater the global needs of industry and society.

MISSION STATEMENT OF THE SCHOOL OF ELECTRONICSENGINEERING

- Create and maintain an environment to excel in teaching, learning and applied research in the fields of electronics, communication engineering and allied disciplines which pioneer for sustainable growth.
- Equip our students with necessary knowledge and skills which enable them to be lifelong learners to solve practical problems and to improve the quality of human life.

M. Tech. VLSI Design

PROGRAMME EDUCATIONAL OBJECTIVES (PEOs)

1. Graduates will be engineering practitioners and leaders, who would help solve industry's technological problems.

2. Graduates will be engineering professionals, innovators or entrepreneurs engaged in technology development, technology deployment, or engineering system implementation in industry.

3. Graduates will function in their profession with social awareness and responsibility.

4. Graduates will interact with their peers in other disciplines in industry and society and contribute to the economic growth of the country.

5. Graduates will be successful in pursuing higher studies in engineering or management.

6. Graduates will pursue career paths in teaching or research.

M. Tech. VLSI Design

PROGRAMME OUTCOMES (POs)

PO_01: Having an ability to apply mathematics and science in engineering applications.

PO_02: Having an ability to design a component or a product applying all the relevant standards and with realistic constraints, including public health, safety, culture, society and environment

PO_03: Having an ability to design and conduct experiments, as well as to analyse and interpret data, and synthesis of information

PO_04: Having an ability to use techniques, skills, resources and modern engineering and IT tools necessary for engineering practice

PO_05: Having problem solving ability- to assess social issues (societal, health, safety, legal and cultural) and engineering problems

PO_06: Having adaptive thinking and adaptability in relation to environmental context and sustainable development

PO_07: Having a clear understanding of professional and ethical

responsibility

PO_08: Having a good cognitive load management skills related to project management and finance

M. Tech. VLSI Design

PROGRAMME SPECIFIC OUTCOMES (PSOs)

On completion of M. Tech. (VLSI Design) programme,
graduates will be able to

PSO1: Apply advanced concepts in Physics of semiconductor devices to design VLSI Systems.

PSO2: Design ASIC and FPGA based systems using industry standard tools.

PSO3: Solve research gaps and provide solutions to socio-economic, and environmental problems.

Master of Technology in VLSI Design

School of Electronics Engineering

Programme Credit Structure	Credits
Discipline Core Courses	**24**
Skill Enhancement Courses	**05**
Discipline Elective Courses	**12**
Open Elective Courses	**03**
Project/ Internship	**26**
Total Graded Credit Requirement	**70**

Discipline Core Courses — 24

		L	T	P	C
MVLD501L	Physics of VLSI Devices	3	0	0	3
MVLD502L	Digital IC Design	3	0	0	3
MVLD503L	Digital Design with FPGA	2	0	0	2
MVLD503P	Digital Design with FPGA Lab	0	0	2	1
MVLD504L	Analog IC Design	3	0	0	3
MVLD504P	Analog IC Design Lab	0	0	2	1
MVLD505L	ASIC Design	3	0	0	3
MVLD505P	ASIC Design lab	0	0	2	1
MVLD506L	VLSI Testing and Testability	3	0	0	3
MVLD506P	VLSI Testing and Testability	0	0	2	1
MVLD507L	IC Technology	3	0	0	3

Skill Enhancement Courses — 05

MENG501P	Technical Report Writing	0	0	4	2
MSTS501P	Qualitative Skills Practice	0	0	3	1.5
MSTS502P	Quantitative Skills Practice	0	0	3	1.5

Discipline Elective Courses — 12

MVLD601L	Computer Aided Design for VLSI	3	0	0	3
MVLD602L	Low Power IC Design	3	0	0	3
MVLD603L	VLSI Verification Methodologies	3	0	0	3
MVLD606L	Mixed Signal IC Design	3	0	0	3
MVLD607L	RFIC Design	3	0	0	3
MVLD608L	VLSI Digital Signal Processing	3	0	0	3
MVLD610L	Nanoscale Devices and Circuit Design	3	0	0	3
MVLD611L	Advanced Computer Architecture	3	0	0	3
MVLD613L	System Design with FPGA	3	0	0	3
MVLD616L	Scripting Languages for Electronic Design Automation	3	0	0	3
MVLD617L	Neuromorphic Engineering and Hardware Accelerators	3	0	0	3
MEDS601L	Electromagnetic Interference and Compatibility	3	0	0	3
MEDS616L	Machine Leaning and Deep Learning	3	0	0	3
MEDS501L	Embedded System Design	3	0	0	3

Open Elective Courses — 03

Engineering Disciplines | Social Sciences

Project and Internship — 26

MVLD696J	Study Oriented Project	02
MVLD697J	Design Project	02
MVLD698J	Internship I/ Dissertation I	10
MVLD699J	Internship II/ Dissertation II	12

Course Code	Course Title	L	T	P	C
MVLD501L	Physics of VLSI Devices	3	0	0	3
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives:

1. Expound the fundamentals of intrinsic, extrinsic semiconductors with carrier concentration, Modeling and physics of various carrier current transport and tunneling mechanisms.
2. Introduce detailed physics and modeling of PN Junction, MOS capacitors, and MOSFETs
3. Review and discuss in detail the short channel effects and the issues of deep sub-micron (DSM) and ultra-deep sub-micron technology (UDSM) transistors
4. Physics of multi-gate transistors.

Course Outcomes:

At the end of the course the student will be able to

1. Design extrinsic semiconductors with specific carrier concentrations, understand the band Structure and diagrams of semiconductors.
2. Calculate and model the carrier transport mechanism in semiconductors
3. Design of PN- junctions for given specifications
4. Understand the Physics of MOS capacitors, MOSFETs and compact models of MOSFETs
5. Understand the short channel effects in DSM and UDSM technology
6. Understand the concept of multi-gate transistors and design of DSM and UDSM transistors to mitigate the short channel effects

Module:1	Semiconductor Physics	5 hours

Energy bands in solids - Intrinsic and Extrinsic semiconductors - Direct and Indirect bandgap -Density of states - Fermi distribution -Free carrier densities - Boltzmann statistics - Thermal equilibrium- Generation and Recombination of carriers

Module:2	Carrier Transport in Semiconductors	4 hours

Current flow mechanisms: Drift current, Diffusion current - Mobility of carriers - Current density equations - Continuity equation.

Module:3	P-N Junctions	5 hours

Thermal equilibrium physics - Energy band diagrams - Space charge layers - Poisson equation - Electric fields and Potentials - p-n junction under applied bias - Static current-voltage characteristics of p-n junctions - Breakdown mechanisms (Zener Breakdown-Tunneling mechanism and Avalanche Breakdown-hot carrier effect)

Module:4	MOS Capacitor	8 hours

Accumulation - Depletion - Strong inversion - Threshold voltage - Contact potential - Gate work function - Oxide and Interface charges - Body effect - C-V characteristics of MOS

Module:5	MOSFETs and Compact Models	8 hours

Drain current - Saturation voltage - Sub-threshold conduction - Effect of gate and drain voltage on carrier mobility - Compact models for MOSFET and their implementation in SPICE: Level 1, 2 and 3 - MOS model parameters in SPICE.

Module:6	Scaling and Short Channel Effects	6 hours

Constant Electric Field scaling and constant Power supply scaling, Effect of scaling - Channel length modulation - Punch-through - Hot carrier degradation - MOSFET breakdown - Drain-induced barrier lowering.		
Module:7	**Deep sub-micron (DSM) and Ultra Deep Sub-Micron (UDSM) Transistor Design Issues**	**7 hours**
Effect of oxide thickness (t_{ox}) - Effect of high-k and low-k dielectrics on the gate leakage and Source and drain leakage - tunnelling effects - Different gate structures (Double gate, Trigate etc.) in DSM and UDSM - Impact and reliability challenges in DSM and UDSM, SOI MOSFETs and FINFETs.		
Module:8	**Contemporary Issues**	**2 hours**
Guest lectures from Industries and R&D Organizations		
	Total Lecture hours:	**45 hours**

Text Book(s)	
1.	Ben G. Streetman and S. Banerjee, Solid State Electronic Devices, 2018, Seventh Edition, Pearson Education.
2	Donald A. Neamen ,Semiconductor Physics and Devices, Basic Principles, 2017, Seventh Edition, McGraw-Hill Education
Reference Books	
1.	Y.P. Tsividis and Colin McAndrew, Operation and Modelling of the MOS Transistor, 2011, Third Edition, Oxford University Press, U.S.
2	Introduction to Semiconductor Materials and devices by M.S Tyagi, John Wiley & Sons, 5th Edition, 2005.
3	J.P. Colinge and C. A. Colinge, Physics of Semiconductor Devices, 2017, Kluwer Academic Publishers, U.S.
4	J.P. Colinge, FinFETs and other multi-gate Transistors, 2020, Springer.

Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test			
Recommended by Board of Studies	07-06-2023		
Approved by Academic Council	No. 70	Date	24-06-2023

Course Code	Course Title	L	T	P	C
MVLD502L	Digital IC Design	3	0	0	3
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives

The course is aimed to

1. Apply the models for state-of-the-art VLSI components, fabrication steps, and hierarchical design flow.
2. Focus on the systematic analysis and design of basic digital integrated circuits in CMOS technology.
3. Enhance problem solving and creative circuit design techniques.
4. Emphasize on the layout design of various digital integrated circuits.
5. Focus on the methodologies and design techniques related to digital integrated circuits.

Course Outcomes

At the end of the course the student will be able to

1. Understand design metric and MOS physics
2. Design layout for various digital integrated circuits.
3. Design the CMOS inverter with optimized power, area and timing.
4. Design static and dynamic digital CMOS circuits.
5. Understand the timing concepts in latch and flip-flops.
6. Design CMOS memory arrays, understand interconnect and clocking issues.

Module:1	Introduction	4 hours

Issues in Digital IC Design- Quality Metrics of a Digital Design – Review of MOS Transistor Theory

Module:2	CMOS Fabrication and Layout	6 hours

CMOS Process Technology N-well, P-well process, Stick diagram for Boolean functions, Optimization using Euler Theorem, Layout Design Rules

Module:3	The CMOS Inverter	6 hours

Static CMOS Inverter- Static and Dynamic Behavioural Practices of CMOS Inverter – Noise Margin. Components of Energy and Power – Switching -Short-Circuit and Leakage Components. Technology scaling and its impact on the inverter metrics - Passive and Active Devices.

Module:4	Performance estimation of Static & Dynamic CMOS Design	8 hours

Designing Fast CMOS Circuits -Logical Effort, Complementary CMOS -Ratioed Logic (Pseudo NMOS, DCVSL) - Pass Transistor Logic - Transmission gate logic - Dynamic Logic Design Considerations - Speed and Power Dissipation of Dynamic logic -Signal integrity issues -Domino Logic.

Module:5	CMOS Sequential Logic Circuit Design	6 hours

Introduction - Static Latches and Registers - Dynamic Latches and Registers - Pulse Based Registers - Sense Amplifier based registers -Latch vs. Register based pipeline structures. Setup and Hold time calculation.

Module:6	Designing Memory & Array structures	7 hours

SRAM and DRAM Memory Core - memory peripheral circuitry – (Memory Cell Stability)-Memory reliability and yield - Power dissipation in memories. (Memory Design issues and Challenges, Various Memory bit cell and design metrics)

Module:7	Interconnects and Datapath Structures	6 hours

Resistive, Capacitive and Inductive Parasitics - Computation of R, L and C for given interconnects - Capacitance and Reliability -Resistance and Reliability - The Full Adder: Circuit Design Considerations - Barrel Shifter - Power and Speed Trade-off's in Datapath Structures.		
Module:8	**Contemporary Issues**	**2 hours**
Guest lecture from Industries and R & D Organizations		
	Total Lecture hours:	**45 hours**
Text Book(s)		
1.	Jan M. Rabaey, AnanthaChadrakasan and BorivojeNikolic, Digital Integrated Circuits: A Design Perspective, 2016, Second Edition, PHI.	
2.	Neil.H, E.Weste, David Harris and Ayan Banerjee, CMOS VLSI Design: A Circuit and Systems Perspective, 2015, Fourth Edition, Pearson Education.	
Reference Books		
1.	Sung-Mo Kang, Yusuf Leblebici, CMOS Digital Integrated Circuits - Analysis and Design, 2014, Fourth Edition, McGraw-Hill.	
2.	Sorab K Gandhi, VLSI Fabrication Principles: Si and GaAs, 2010, Second Edition, John Wiley and Sons.	
3	Ivan Sutherland, R. Sproull and D. Harris, "Logical Effort: Designing Fast CMOS Circuits", 1999, Publisher: Morgan Kaufmann	
5	Andrei Pavlov, Manoj Sachdev, "CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies: Process-Aware SRAM Design and Test" ,2008, Springer	
6	Jawar Singh, Saraju P. Mohanty, Dhiraj K. Pradhan, "Robust SRAM Designs and Analysis", 2013, Springer-Verlag New York	
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test.		
Recommended by Board of Studies	07-06-2023	
Approved by Academic Council	No. 70	Date 24-06-2023

Course Code	Course Title	L	T	P	C
MVLD503L	Digital Design with FPGA	2	0	0	2
Pre-requisite	NIL	Syllabus Version			
		1.0			

Course Objectives

This course is aimed to

1. Understand the various abstraction level in Verilog HDL.
2. Model the complex combinational and sequential circuits with Verilog HDL
3. Provide in depth understanding of state machine design and modeling using Verilog HDL.
4. Understand about different FPGA Architecture like Xilinx and ALTERA and RAM and controller design.

Course Outcomes

After completion of the course the student will be able to:

1. Design and implement digital circuits using Data Flow & Structural Modeling.
2. Design and develop combinational circuits using data flow approach
3. Design and implement sequential digital circuits using Behavioral Modeling.
4. Understand and develop data-path and controller design
5. Develop and test memory sub-system.
6. Build digital designs using FPGA.

Module:1	**Verilog HDL – Data Flow & Structural Modeling**	**6 hours**
Verilog Fundamentals - Operators - Gate Level Modeling - Data Flow Modeling - Test Bench.		
Module:2	**Design and Modeling of Combinational Circuits**	**4 hours**
Ripple carry Adders – Carry look ahead adder – Unsigned binary Multipliers. Synthesizable Coding Style for Combinational Circuits.		
Module:3	**Verilog HDL – Behavioral Modeling**	**4 hours**
Behavioral level Modeling- Procedural Assignment Statements- Blocking and Non-Blocking Assignments -Tasks & Functions - System Tasks & Compiler Directives		
Module:4	**Design and Modeling of Sequential Circuits**	**4 hours**
FSM modeling of Sequence detector - Serial adder - Vending machine. Synthesizable Coding Style for Sequential Circuits and FSM.		
Module:5	**Design and Modeling of Datapath and Controller logic**	**3 hours**
Case Study: Binary Counter - Bus Protocol		
Module:6	**Modeling of FIFO and Memory**	**3 hours**
Synchronous and Asynchronous FIFO – Single port and Dual port ROM and RAM		
Module:7	**FPGA Architecture**	**4 hours**
Types of Programmable Logic Devices: PLA, PAL, CPLD - FPGA Architecture - Programming Technologies-Chip I/O- Programmable Logic Blocks- Fabric and Architecture of FPGA - Xilinx / Intel / Actel FPGA Architecture – Case Study		
Module:8	**Contemporary Issues**	**2 hours**
Guest lecture from Industries and R & D Organizations		
	Total Lecture hours:	**30 hours**

Text Book(s)

1.	Michael D Ciletti, Advanced Digital Design with the Verilog HDL, 2017, Second Edition, Pearson Education.

2.	Ming-Bo Lin, Digital Systems Design and Practice: Using Verilog HDL and FPGAs, 2015, Second Edition, Create Space Independent Publishing Platform.
Reference Books	
1.	Wayne Wolf, FPGA Based System Design, 2011, Prentices Hall Modern Semiconductor Design Series.
2.	Charles H Roth Jr, Lizy Kurian John and Byeong Kil Lee, Digital Systems Design using Verilog, 2016, First Edition, Cengage Learning.

Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test			
Recommended by Board of Studies	07-06-2023		
Approved by Academic Council	No. 70	Date	24-06-2023

Course Code	Course Title	L	T	P	C
MVLD503P	Digital Design with FPGA Lab	0	0	2	1
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives

This course is aimed to

1. Model the complex combinational and sequential circuits using Verilog HDL

Course Outcome

After completion of the course the student will be able to:

1. Design and optimize complex combinational and sequential digital circuits using Verilog.
2. Implement the designed digital design using FPGA.

	Indicative Experiments	
1.	Many ink-jet printers have six cartridges for different colored ink: black, cyan, magenta, yellow, light cyan and light magenta. A multibit signal in such a printer indicates selection of one of the colors. Write a data flow Verilog model for a decoder for use in the inkjet printer described above. The decoder has three input bits representing the choice of color cartridge and six output bits, one to select each cartridge. Verify the output of the design using test bench by simulating in Modelsim Simulator. Implement the design in ALTERA DE2-115 Board and verify it's functionality.	4 hours
2.	Write a behavioral Verilog code to divide the ALTERA DE2-115 Board clock frequency 50MHz by 40MHZ, 30MHz, 20 MHz, 10MHz. Display each of the output using LEDs available in the board.	4 hours
3.	Design and implement a circuit on the DE2-115 board that acts as a time-of-day clock. It should display the hour (from 0 to 23) on the 7-segment displays HEX7−6, the minute (from 0 to 60) on HEX5−4 and the second (from 0 to 60) on HEX3−2. Use the switches SW15−0 to preset the hour and minute parts of the time displayed by the clock.	4 hours
4.	We wish to implement a finite state machine (FSM) that recognizes two specific sequences of applied input symbols, namely four consecutive 1s or four consecutive 0s. There is an input w and an output z. Whenever w = 1 or w = 0 for four consecutive clock pulses the value of z has to be 1; otherwise, z = 0. Overlapping sequences are allowed, so that if w = 1 for five consecutive clock pulses the output z will be equal to 1 after the fourth and fifth pulses. Design and Implement the design using DE2-115 Board.	8 hours
5.	Write a behavioral Verilog code to design FIFO with the following specification d_in: input data; 8 bit width is considered d_out: output data; 8 bit width is considered · w_en: write enable signal r_en: read enable signal r_next_en: read next enable w_next_en: write next enable w_clk: write clock; 10 MHz for this design r_clk: read clock; 50 MHz for this design w_ptr: write address pointer; 4 bit to address depth of 16 · r_ptr: read address pointer; 4 bit to address depth of 16 · ptr_diff: address pointer difference; 4 bit width f_full_flag: FIFO full flag; asserted when FIFO is full · f_empty_flag: FIFO empty flag; asserted when FIFO is empty Use Dual Port RAM available in ALTERA IP library to realize the FIFO. Implement the design using ALTERA DE2-115 board.	10 hours

		Total Laboratory Hours	**30 hours**
Mode of Assessment: Continuous Assessment and Final Assessment Test			
Recommended by Board of Studies	28-07-2022		
Approved by Academic Council	No. 67	Date	08-08-2022

Course Code	Course title	L	T	P	C
MVLD504L	Analog IC Design	3	0	0	3
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives

The course is aimed to

1. Analyze and design single-ended and differential IC amplifiers.
2. Understand the relationships between devices, circuits and systems.
3. Emphasize the design of practical amplifiers, small systems and their design parameter trade-offs.

Course Outcomes

At the end of the course the student will be able to

1. Analyze low-frequency characteristics of single-stage amplifiers and differential amplifiers
2. Analyze high-frequency response and noise of amplifiers.
3. Understand the feedback concepts.
4. Analyze and design of high gain amplifiers.
5. Understand stability analysis and frequency compensation techniques of amplifiers.
6. Understand Bandgap reference circuits and PMICs.

Module:1	Current source and Amplifier design:	7 hours

MOS Device models, MOS Current Sources and Sinks, Current Mirror: Basic Current Mirrors, Cascode current Mirrors. Single stage Amplifies: Basic concepts, Common Source stage, Common Gate stage, Cascode stage. Differential stage: Single ended and Differential operation. Basic Differential Pair.

Module:2	Frequency response and Noise analysis of Amplifiers:	8 hours

Miller effect, Frequency response of Common Source stage, Common Gate stage, Cascode stage and Differential pair. Noise in Amplifiers: Common Source stage, Common Gate stage, Cascode stage, Differential pair. Noise Bandwidth.

Module:3	Feedback Amplifiers:	7 hours

Ideal feedback equation, Gain sensitivity, Effect of Negative Feedback on Distortion, Types of Feedback Amplifiers. Feedback configurations: voltage-voltage, current-voltage, current-current, voltage-current feedback. Practical configurations and Effect of loading.

Module:4	Operational Amplifier	6 hours

Need for Single and Multistage amplifiers – Telescopic, Folded, Gain boosting, Two stage Op Amps, Performance Analysis: DC gain, Frequency response, Slew rate, Common mode Feedback, Common Mode Rejection Ratio, Power Supply Rejection Ratio.

Module:5	Stability and Frequency Compensation	7 hours

Basic Concepts, Multipole Systems, Gain Margin, Phase Margin, Frequency Compensation: – Dominant pole, Miller Compensation, Compensation of Miller RHP Zero, Nested Miller Compensation, Reversed Nested Miller Compensation, Stability Criterion- Nyquist and Root Locus.

Module:6	Bandgap References	4 hours

Supply-Independent Biasing, Temperature-Independent References, PTAT Current Generation, Constant-*Gm* Biasing

Module:7	**Phase Locked Loops**	**4 hours**
Problem of Lock acquisition, Phase Detector, Basic PLL and its dynamics, Charge-pump PLL, Non-ideal effects in PLL: PFD/CL non idealities, Jitter, Delay Locked Loop, Applications.		
Module:8	**Contemporary Issues**	**2 hours**
Guest lecture from Industries and R & D Organizations		
	Total Lecture hours:	**45 hours**

Text Book(s)	
1.	Behzad Razavi, Design of Analog CMOS Integrated Circuits, 2017, Second Edition, McGraw-Hill.
2.	Behzad Razavi, "Design of CMOS Phase-Locked Loops", Cambridge University Press, 2020.
Reference Books	
1.	Phillip E. Allen and Douglas R. Holberg, CMOS Analog Circuit Design, 2010, Second Edition, Oxford University Press, UK.
2.	R. Jacob Baker, CMOS Circuit Design, Layout and Simulation, 2010, Third Edition, IEEE Press Series on Microelectronic Systems, Wiley Publications.

Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test.			
Recommended by Board of Studies	07-06-2023		
Approved by Academic Council	No. 70	Date	24-06-2023

Course Code	Course Title	L	T	P	C
MVLD504P	Analog IC Design Lab	0	0	2	1
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives

The course is aimed to

1. Analyze and design single-ended and differential IC amplifiers.
2. Understand the relationships between devices, circuits and systems.
3. Emphasize the design of practical amplifiers, small systems and their design parameter trade-offs.

Course Outcome

At the end of the course students will be able to

1. Design and characterize amplifiers, Low Dropout Regulator according to design specifications in industry standard EDA tool.

Indicative Experiments

1.	Simulation of MOSFET IV Characteristics, Second order parameters	2 hours
2.	CMOS Inverter - DC, AC, Transient Analysis, Post layout simulation	2 hours
3.	Design of Basic Single Stage Amplifiers (Common Source, Common Gate and Common Drain)	4 hours
4.	Analysis and Design of Simple Current Mirror and Cascode Current Mirror.	4 hours
5.	Analysis and Design of Differential Amplifier with Active load and Current Source Load.	4 hours
6.	Layout of Differential Amplifier	6 hours
7.	Analysis and Design of Cascode Amplifier and Suggest a Circuit to overcome Voltage Headroom Limitation.	4 hours
8.	Analysis and Design of Two-Stage Opamp with Frequency Compensation.	4 hours
	Total Laboratory Hours	**30 hours**

Mode of Evaluation: Mode of Assessment: Continuous Assessment and Final Assessment Test

Recommended by Board of Studies	07-06-2023		
Approved by Academic Council	No. 70	Date	24-06-2023

Course Code	Course Title	L	T	P	C
MVLD505L	ASIC Design	3	0	0	3
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives

The course aimed to

1. Understand the RTL synthesis Flow with respect to different cost functions.
2. Analyse Static Timing requirements for ASIC design.
3. Discuss the guidelines at each abstraction level in physical design.
4. Understand the importance of physical design verification.

Course Outcomes

At the end of the course the student will be able to

1. Synthesize the given design by considering various constraints and optimize the same.
2. Understanding the logical equivalence checking.
3. Understand various timing parameters and perform Static Timing Analysis for ASIC design.
4. Compare OCV modelling techniques.
5. Perform physical design by adhering to guidelines.
6. Understand the importance of physical design verification.

Module:1	ASIC Design Methodology & Design Flow	4 hours

Implementation Strategies for Digital ICs: Custom IC Design- Cell-based Design Methodology - Array based implementation approaches - Traditional and Physical Compiler based ASIC Flow.

Module:2	RTL Synthesis	6 hours

RTL synthesis Flow – Synthesis Design Environment & Constraints – Architecture of Logic Synthesizer - Technology Library Basics– Components of Technology Library –Synthesis Optimization- Technology independent and Technology dependent synthesis- Data path Synthesis – Low Power Synthesis

Module:3	Formal Verification	6 hours

Combinational Equivalence Checking- Constrained EC - Cut Point-Based EC - Sequential Equivalence Checking - Register Correspondence - Model Checking - Property Checking

Module:4	Basic Timing Analysis	7 hours

Timing Parameter Definition – Setup Timing Check- Hold Timing Check- Multicycle Paths- Half-Cycle Paths- False Paths

Module:5	Advanced Timing Analysis	7 hours

Clock skew optimization – On-Chip Variations- AOCV-POCV-Time Borrowing- Setup and Hold Violation Fixing. Origins of Clock Skew/Jitter and impact on Performance. Clock Domain Crossing – Synchronizers.

Module:6	Physical Design	8 hours

Detailed steps in Physical Design Flow- Guidelines for Floor plan, Placement, CTS and routing– ECO flow – Signal Integrity Issues.

Module:7	Physical Design Verification	5 hours

Timing Sign-off, Physical Verification – Signoff DRC and LVS, ERC, IR Drop Analysis, Antenna Check, Electro-Migration Analysis and ESD Analysis.

Module:8	Contemporary Issues	2 hours

Guest lecture from Industries and R & D Organizations		
	Total Lecture hours:	**45 hours**
Text Book(s)		
1.	Vaibbhav Taraate, ASIC Design and Synthesis RTL Design Using Verilog, 2021, First Edition, Springer, Singapore.	
2.	J. Bhasker and Rakesh Chadha, Static Timing Analysis for Nanometer Designs, 2010, First Edition, Springer, USA.	
Reference Books		
1.	Khosrow Golshan, PHYSICAL DESIGN ESSENTIALS An ASIC Design Implementation Perspective, 2010, First Edition, Springer.	
2.	Michael John Sebastian Smith, Application-Specific Integrated Circuits, 2002, First Edition, Addison Wesley.	
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test		
Recommended by Board of Studies	07-06-2023	
Approved by Academic Council	No. 70	Date 24-06-2023

Course Code	Course Title	L	T	P	C
MVLD505P	ASIC Design Lab	0	0	2	1
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives

The course is aimed to

1. To apply theoretical knowledge gained in the ASIC Design course and get hands-on experience of the topics.

Course Outcome

At the end of the course the student will be able to

1. Design, simulate and synthesize complex digital system
2. Analyse and fix the timing violations
3. Design ASIC based digital systems using industry standard EDA tools.

Indicative Experiments		
1.	Design of Digital Architecture for given specification	6 hours
2.	Logical Synthesis of Digital Architecture	6 hours
3.	Netlist Optimization, GLS and Formal Verification	6 hours
4.	Physical Synthesis of Digital Architecture	6 hours
5.	Physical Verification of Digital Architecture	6 hours
	Total Laboratory Hours	**30 hours**

Mode of Assessment: Continuous Assessment and Final Assessment Test

Recommended by Board of Studies	28-07-2022		
Approved by Academic Council	No. 67	Date	08-08-2022

Course Code	Course Title	L	T	P	C
MVLD506P	VLSI Testing and Testability Lab	0	0	2	1
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives

The course is intended to

1. Introduce the concept of modeling and simulation of logic and memory testing
2. Familiarize different design for testability techniques for improving the yield of IC design using industry standard EDA tools

Course Outcomes:

After completion of the course the student will be able to:

1. Generate test patterns and perform fault simulation for digital logic and memory circuits.
2. Apply DFT techniques viz. scan based testing, BIST and boundary scan for improving testability using EDA tools.

Indicative Experiments		
1.	Fault Simulation and Test generation for combination circuits	4 hours
2.	Clock and reset rule check at RTL	4 hours
3.	Scan Chain Insertion, DRC and ATPG	2 hours
4.	At-Speed Patterns and On-Chip Clock Controllers (LoS and LoC)	4 hours
5.	Advanced fault modeling	2 hours
6.	SDF annotated simulation	4 hours
7.	Boundary scan test	4 hours
8.	Testing of memories (BIST insertion, validation and BIST repair)	6 hours
	Total Laboratory Hours	**30 hours**

Mode of Assessment: Continuous Assessment and Final Assessment Test

Recommended by Board of Studies	28-07-2022		
Approved by Academic Council	No. 67	Date	08-08-2022

Course Code	Course Title	L	T	P	C
MVLD506L	VLSI Testing and Testability	3	0	0	3
Pre-requisite	NIL	Syllabus Version			
		1.0			

Course Objectives :

The course is intended to

1. Introduce the concept of modeling and simulation of logic and memory testing.
2. Familiarize different design for testability techniques for improving the yield of IC design.

Course Outcomes :

After completion of the course students will be able to

1. Understand the Fault Models and generate test patterns for digital circuits.
2. Apply DFT techniques viz. scan based testing, BIST and boundary scan for improving testability
3. Use of test vector compression and test response compaction techniques to reduce test time and memory storage
4. Test, diagnose and repair memory faults in SoC

Module:1	VLSI Testing and Fault Modelling	6 hours

Importance of Testing - Testing during the VLSI Lifecycle - Challenges in the VLSI Testing: Test Generation - Fault Models – Levels of Abstraction in VLSI Testing - Historical Review of VLSI Test Technology - Fault Equivalence - Fault Dominance - Fault Collapsing - Check point Theorem.

Module:2	Fault Simulation and Test Generation	5 hours

Fault Simulation: Serial, Parallel, Deductive, Concurrent, Fault sampling - Combinational Test Generations -ATPG for Combinational Circuits - D-Algorithm – Classification of faults.

Module:3	Design for Testability	7 hours

Testability Analysis: SCOAP measures for Combinational Circuits - Design for Testability Basics - Ad Hoc Approach - Structured Approach - Scan Cell Designs - Scan Architectures - Scan Design Rules - Scan Design Flow – Special Purpose Scan Designs

Module:4	Logic Built-in Self-Test	7 hours

BIST Design Rules - Test Pattern Generation: Exhaustive Testing, Pseudo-Random Testing, Pseudo-Exhaustive Testing, Delay Fault Testing - Output Response Analysis - Logic BIST Architectures

Module:5	Test Compression and Boundary scan	6 hours

Test Stimulus Compression Techniques: Linear-Decompression-Based Schemes – Broadcast based compression schemes. Test Response Compaction - Digital Boundary Scan (IEEE Std. 1149.1): Test Architecture and Operations - On-Chip Test Support with Boundary Scan - Board and System-Level Boundary-Scan Control Architectures – IJTAG architectures.

Module:6	Memory Testing and Built-In Self-Test	6 hours

RAM Functional Fault Models and Test Algorithms - RAM Fault Simulation and Test Algorithm Generation - Memory Built-In Self-Test

Module:7	Memory Diagnosis and Built-In Self-Repair	6 hours

BIST with Diagnostic Support - RAM Defect Diagnosis and Failure Analysis - Built-In Self-Repair

Module:8	Contemporary Issues	2 hours

	Total Lecture hours:	**45 hours**

Text Book(s)	
1.	Laung-Terng Wang, Cheng-Wen Wu, and Xiaoqing Wen, VLSI Test Principles and Architectures, 2013, The Morgan Kaufmann.
2.	M. Bushnell, Vishwani Agrawal - Essentials of Electronic Testing for Digital, Memory, and Mixed-Signal VLSI Circuits, 2006, Springer.
Reference Books	
1.	Laung-Terng Wang, Charles E. Stroud, Nur A. Touba, "System-on-chip Test Architectures: Nanometer Design for Testability", 2008, Morgan Kaufmann Publishers.
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test	

Recommended by Board of Studies	28-07-2022		
Approved by Academic Council	No. 67	Date	08-08-2022

Course Code	Course Title	L	T	P	C
MVLD507L	IC Technology	3	0	0	3
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives

The course is intended to

1. Introduce the process involved in semiconductor manufacturing, lithography and fabrication.
2. Model the oxidation growth rate, to understand oxidation process, diffusion process and to expound the Ion Implantation process.
3. Explain the thin film deposition process and review the differences between MOS and Bipolar Process Integration.

Course Outcomes

At the end of the course the student will be able to

1. Understand & Analyze the process involved in semiconductor manufacturing, lithography and fabrication.
2. Understand & Evaluate the various lithography techniques used for pattern transfer.
3. Analyze the diffusion and ion implantation mechanism in semiconductors.
4. Apply models for understanding the oxide growth
5. Analyze the process involved in thin film deposition and etching.
6. Evaluate the difference between MOS and Bipolar Process

Module:1	Crystal Growth	5 hours

Introduction to Semiconductor Manufacturing and Fabrication, Clean Room types and Standards, Crystal Structures, Defects in Crystals, Physics of the Crystal growth, Process flow, wafer fabrication and basic properties of silicon wafers.

Module:2	Lithography	7 hours

The Photolithographic Process, Photomask Fabrication, Comparison between positive and negative photoresists, Exposure Systems, Characteristics of Exposure Systems, E-beam Lithography, X- ray lithography

Module:3	Oxidation	6 hours

The Oxidation Process, Modeling Oxidation, Masking Properties of Silicon Dioxide, Technology of Oxidation, Si-SiO_2 Interface

Module:4	Diffusion and Ion Implantation	6 hours

The Diffusion Process, Mathematical Model for Diffusion Constant, The Diffusion Coefficient, Successive Diffusions, Diffusion Systems, Implantation Technology, Mathematical Model for Ion Implantation, Selective Implantation, Channeling, Lattice Damage and Annealing, Shallow Implantations.

Module:5	Thin film deposition, contacts, packaging and yield	9 hours

Chemical Vapor Deposition, Physical Vapor Deposition, Epitaxy, Metal Interconnections and Contact Technology, Silicides and Multilayer-Contact Technology, Copper Interconnects and Damascene Processes, Passivation techniques, Wafer Thinning and Die Separation, Die Attachment, Wire Bonding, Packages, Yield

Module:6	Etching	6 hours

Isotropic and Anisotropic, Selectivity, Wet and Dry etching – Reactive Ion Etching-CMP.

Module:7	**Process Integration for Advanced Devices**	**4 hours**
FinFETs, Compound Semiconductor (III-V) based devices		
Module:8	**Contemporary Issues**	**2 hours**
Guest lecture from Industries and R & D Organizations		
	Total Lecture hours:	**45 hours**

Text Book(s)	
1.	S.M. Sze, VLSI technology, 2017, Second Edition, Tata McGraw-Hill.
2.	James D. Plummer, Michael Deal and Peter D. Griffin, "Silicon VLSI Technology: Fundamentals, Practice and Modelling", April 2020, Prentice Hall Electronics and VLSI Series.
Reference Books	
1.	S.A. Campbell, The science and engineering of microelectronics fabrication, 2012, Second Edition, Oxford University Press, UK.
2.	Simon M. Sze, Gary S. May, Fundamentals of Semiconductor Fabrication, 2011, Wiley.
3.	R.C. Jaeger, Introduction to microelectronic fabrication, 2013, Second Edition, Prentice Hall.

Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test			
Recommended by Board of Studies	07-06-2023		
Approved by Academic Council	No. 70	Date	24-06-2023

Course Code	Course Title	L	T	P	C
MVLD601L	Computer Aided Design For VLSI	3	0	0	3
Pre-requisite	NIL	Syllabus Version			
		1.0			

Course Objectives

The course is aimed to

1. Acquire the fundamentals of graphs, the relevance and, their applications to VLSI design automation and introduce the estimation of computational complexity and the general classes of computational problems.
2. Explain With relevant examples and algorithms demonstrate partitioning, floor planning,area routing, clock routing and pin assignment of physical design flow.
3. Introduce the students to machine learning concepts in physical design.

Course Outcomes

At the end of the course students will be able to

1. Develop the graphs for the given problems; determine and analyse the computational complexity of physical design algorithms.
2. Create the partition for a given design.
3. Develop and change the floorplans in an abstract manner and use computer algorithms tomake large and optimized floorplans
4. Create optimized placements on the silicon chip and perform complex routing usingalgorithms and computer codes.
5. Design clock trees to distribute the clock signals on the chip while satisfying variousconstraints like clock skew and wire length.
6. Understand machine learning concepts in computer aided design for VLSI.

Module:1	Graph theory and Computational complexity of algorithms	6 hours

Y Chart- Physical design top down flow- Review of graph theory: complete graph, connectedgraph, sub graph, isomorphism, bi partite graph tree. Big-O notation- Class P- class NP -NP-hard- NP-complete.

Module:2	Partitioning	7 hours

Problem formulation- Group Migration Algorithm: Kernighan-Lin Simulated annealing basedPartitioning.

Module:3	Floor planning	6 hours

Stock Meyer algorithm- Wong-Liu algorithm (Normalized polish expression), Sequence pair technique.

Module:4	Pin Assignment and Placement	6 hours

Pin Assignment: Concentric circle mapping, Topological pin assignment- Power and groundrouting. Placement: Wire length estimation models for placement - Quadratic placement

Module:5	Routing	7 hours

Routing: Grid routing- Maze routing- Line Probe algorithms, Weighted Steiner tree approach. Global routing: Rectilinear routing(spanning tree, steiner tree)-Dijkstra's algorithm-routing

Detailed routing: Problem formulation- Two layer channel routing: Left Edge algorithm, Dogleg router- Net Merge channel router - Introduction to switch box

routing.		
Module:6	**Clock Tree Topologies**	**8 hours**
Clocking tree topologies: H-tree, Xtree- Method of Means and Medians (MMM) - recursive geometric matching- Elmore delay model to calculate skew- Buffer insertion in clock trees- Exact Zero skew clock routing algorithm. Clock mesh topologies: uniform and non-uniformmesh.		
Module:7	**Machine Learning in Physical Design**	**3 hours**
Machine Learning for Datapath Placement, Machine Learning for Routability-Driven Placement, Machine Learning for Clock Optimization.		
Module:8	**Contemporary Issues**	**2 hours**
Guest lectures from Industries and R&D Organizations		
	Total Lecture hours:	**45 hours**

Text Book(s)	
1.	Andrew B. Kahng, Jens Lienig, Igor L. Markov, JinHu, VLSI Physical Design: From Graph Partitioning to Timing Closure, 2022, Second edition, Springer International Publishing.
2.	Sung Kyu Lim, Practical Problems in VLSI Physical Design Automation, 2011, Springer, India.
Reference Books	
1.	Rajesh K. Maurya , Ganesh M. Magar, Swati R. Maurya, Graph Theory & Applications, 2016, Technical Publications, India
2.	Brian Christian and Tom Griffiths, Algorithms to Live By: The Computer Science of Human Decisions, 2017, First edition, William Collins, USA.
3.	Elfadel, Ibrahim M., Duane S. Boning, and Xin Li, Machine learning in VLSI Computer-Aided Design, 2019, First edition, Springer, Switzerland.
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and FinalAssessment Test.	

Recommended by Board of Studies	07-06-2023		
Approved by Academic Council	No. 70	Date	24-06-2023

Course Code	Course Title	L	T	P	C
MVLD602L	Low Power IC Design	3	0	0	3
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives:

The course is aimed to

1. To understand the concept of VLSI circuit for low power consumption
2. To design various circuits with optimal power consumption.
3. To get an insight on low power issues and challenges at various design levels.
4. To design a system with multiple supply and threshold voltages applicable for various applications.

Course Outcomes:

At the end of the course the student will be able to:

1. Analyse the need for low power VLSI circuits
2. Apply techniques to estimate power consumption of VLSI circuits.
3. Optimize the power consumption using algorithmic and architectural level approach.
4. Apply logic-level and RTL techniques in various designs to optimize power consumption of the VLSI circuits.
5. Apply various circuit techniques to optimize the power consumption.
6. Analyse and explore the usage of sleep transistors and IP design for low power.

Module:1	Introduction to Low Power Design Methods	4 hours

Motivation- Context and Objectives-Sources of Power dissipation in Ultra Deep Submicron CMOS Circuits – Static, Dynamic and Short circuit components Effects of scaling on power consumption- Low power design flow- Normalized Figure of Merit – PDP& EDP- Overview of power optimization at various levels.

Module:2	Power Estimation	6 hours

Theoretical background – Calculation of Steady state probability, Transition probability, Conditional probability, Transition probability of correlated inputs, Transition density; Estimation of Switching activity, Estimation of glitching power.

Module:3	Algorithmic and Architecture Level Optimization	7 hours

Computer arithmetic techniques for low power. Software level power optimization. Pipelining, Parallel Processing and retiming approaches for power minimization, Multiple supply voltage for low power -MVS,DVS.AVS, DVFS, Optimal drivers of high speed low power ICs,

Module:4	Register Transfer Level Optimization	7 hours

Low power clock-Interconnect and layout designs- Low power memory design and low power SRAM architectures. Pre-computation, Clock gating, Data gating Bus Encoding techniques, Deglitching for low power, Synthesis of FSM for low power

Module:5	Gate and Circuit Level Optimization	6 hours

Transistor variable re-ordering for power reduction, Low power library cell design (GDI). Circuit techniques for reducing power consumption in Adders, Multipliers.

Module:6	Leakage Power Reduction	8 hours

Leakage power reduction techniques-stacking techniques, sleepy keeper technique, super cut off CMOS, VTCMOS, MTCMOS,DTCMOS- energy constrained and delay constrained. Sleep Transistor Design- switch efficiency, area efficiency, IR drop, normal Vs reverse body bias. Inrush current and current latency. Power gating – course grain and fine grain. Isolation, retention, power down and wake up methods.		
Module:7	**Low Power Techniques Automation**	**5 hours**
Low power design techniques automation levels, Power-Aware design flow, Unified power format (UPF): Necessity, UPF tutorial, Low power design example using UPF, Design flow modification with UPF.		
Module:8	**Contemporary Issues**	**2 hours**
Guest lecture from Industries and R & D Organizations		
	Total Lecture hours:	**45 hours**

Text Book(s)	
1.	Kaushik Roy, Sharat Prasad, Low Power CMOS VLSI Circuit Design, 2010, Second edition, John Wiley and Sons Inc,
2.	Ajit Pal , Low Power VLSI circuits and Systems, 2016, First edition, Springer, India,
Reference Books	
1.	Gary K.Yeap, Practical Low Power Digital VLSI Design, 2010, First Edition, Springer, USA.
2.	Jan M.Rabaey, Massoud Pedram, Low power Design methodologies, 2014, First Edition, Springer, US.
3.	Soudris, Dimitrios, Christrian Pignet, Goutis, Costas, Designing CMOS circuits for low power, 2011, First Edition, Springer, USA.
4.	Michael Keating, David Flynn, Robert Aitken, Alan Gibbons, Kaijian Shi, Low power methodology manual: for system-on-chip design, 2007, Springer, New York.
5.	Abdellatif Bellaouar, Mohamed Elmasry, Low-Power Digital VLSI Design: Circuits And Systems, 2019, Springer, New York.
6.	Low Power Digital VLSI Design Circuits and Systems by S. Ramamurthy, Medtec, 1st Edition, June 2014
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test.	

Recommended by Board of Studies	07-06-2023		
Approved by Academic Council	No. 70	Date	24-06-2023

Course Code	Course Title	L	T	P	C
MVLD603L	VLSI Verification Methodologies	3	0	0	3
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives

The course is aimed to

1. To introduce various verification techniques.
2. To write Test bench using System Verilog.
3. To develop UVM test bench environment

Course Outcomes

At the end of the course students will be able to

1. Demonstrate the VLSI verification techniques.
2. Define classes and create objects.
3. Develop design using System Verilog
4. Create Verification environment using System Verilog
5. Perceive the UVM Verification environment.
6. Create reusable verification environment using UVM.

Module:1	**Verification Techniques**	**6 hours**
Introduction to Verification - Testing Vs Verification - Verification Technologies - Functional Verification- Code coverage – Functional coverage. Test bench – Linear Test bench - Linear Random Test bench - Self-checking Test bench – Regression - RTL Formal Verification.		
Module:2	**Basic OOP**	**5 hours**
OOP Terminology, Creating Object, object deallocation, copying objects, static variables, Global variables, Inheritance, Polymorphism		
Module:3	**System Verilog – Data Types & Procedural statements**	**7 hours**
Introduction to System Verilog – Literal values-data Types – Arrays – Array methods – Creating new types with type def – user defined structures – Enumerated types – attributes - operators –expressions - Procedural statements and control flow - Processes in System Verilog – Task and functions – Routine arguments – Returning from a routine		
Module:4	**Connecting Test bench and Design**	**6 hours**
Program, Interface, Stimulus timing, Module interactions, Connecting together, Development of self-checking test environment – Generator, Transactor, Driver, Monitor, Checker, Scoreboard		
Module:5	**Randomization, Assertion and Coverage**	**7 hours**
Randomization in system Verilog, Constraints, Functional coverage, cross coverage, cover groups, Assertions.		
Module:6	**Universal Verification Methodology**	**6 hours**
Introduction to UVM - Verification components - Transaction level modeling		
Module:7	**UVM – Verification Environments**	**6 hours**
Developing reusable verification components - Using Verification components – Developing reusable verification environment – Register classes – Bus Protocol Verification (AHB/APB).		
Module:8	**Contemporary Issues**	**2 hours**
Guest lecture from Industries and R & D Organizations		
	Total Lecture hours:	**45 hours**

Text Book(s)			
1.	Ashok B. Mehta, Introduction to System Verilog, 2021, Springer, New York.		
2.	Srivatsa Vasudevan, Practical UVM Step by Step with IEEE 1800.2, 2020, Second edition, R R Bowker, CA, USA.		
Reference Books			
1.	Vanessa R. Copper, "Getting started with UVM: A Beginner's Guide", 2013, First Edition, Verilab Publishing		
2.	Christian B Spear, "System Verilog for Verification: A guide to learning the Testbench language features", 2012, Third Edition, Springer, USA.		
3.	Janick Bergeron, "Writing Testbenches using System Verilog" 2006, Synopsys Inc., Springer, USA.		
4.	Ray Salmei, "The UVM Primer: A Step-by-Step Introduction to the Universal Verification Methodology" 2013, First Edition, Boston Light Press.		
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test.			
Recommended by Board of Studies	07-06-2023		
Approved by Academic Council	No. 70	Date	24-06-2023

Course Code	Course Title	L	T	P	C
MVLD606L	Mixed Signal IC Design	3	0	0	3
Pre-requisite	MVLD504L	Syllabus version			
		1.0			

Course Objectives:

The course is aimed to

1. Introduce the design aspects of dynamic analog circuits and analog-digital interface electronics in CMOS technology.
2. Specify design implementation of ADC & DAC.

Course Outcomes:

At the end of the course the student will be able to

1. Understand the theory of discrete-time signal processing and its implementation using analog techniques.
2. Design Sample and Hold Circuits using MOS by considering the non-idealities.
3. Analyze CMOS based Switched Capacitor Circuits.
4. Understanding basics of Data Converters.
5. Analyze the architectures of ADCs and DAC.
6. Understand the oversampling converter architecture.

Module:1	**Sampling:**	**5 hours**

Introduction – sampling - Spectral properties of sampled signals - Oversampling – Anti-alias filter design. Time Interleaved Sampling - Ping-Pong Sampling System - Analysis of offset and gain errors in Time Interleaved Sample and Hold.

Module:2	**Sampling Circuits**	**5 hours**

Sampling circuits- Distortion due to switch - Charge injection - Thermal noise in sample and holds - Bottom plate sampling - Gate bootstrapped switch -Nakagome charge pump. Characterizing Sample and hold - Choice of input frequency.

Module:3	**Switched Capacitor Circuits:**	**6 hours**

Switched Capacitor (SC) circuits– Parasitic Insensitive Switched Capacitor amplifiers - Non idealities in SC Amplifiers – Finite gain - DC offset - Gain Bandwidth Product. Fully differential SC circuits - DC negative feedback in SC circuits.

Module:4	**A/D and D/A Converters Fundamentals:**	**5 hours**

Data converter fundamentals: Offset and gain Error - Linearity errors - Dynamic Characteristics – SQNR - Quantization noise spectrum.

Module:5	**Analog to Digital Converter Architectures:**	**7 hours**

Flash ADC - Regenerative latch - Preamp offset correction - Preamp Design - necessity of up-front sample and hold for good dynamic performance. Folding ADC - Multiple-Bit Pipeline ADCs and SAR ADC.

Module:6	**Digital to Analog Converter Architectures:**	**7 hours**

DAC spectra and pulse shapes - NRZ vs RZ DACs. DAC Architectures: Binary weighted - Thermometer DAC - Current steering DAC - Current cell design in current steering DAC - Charge Scaling DAC - Pipeline DAC.

Module:7	**Oversampling Converter:**	**8 hours**

Benefits of Oversampling -Oversampling with Noise Shaping - Signal and Noise Transfer Functions - First and Second Order Delta-Sigma Converters. Introduction to Continuous-time Delta Sigma Modulators - time-scaling - inherent antialiasing property - Excess Loop Delay - Influence of Op-amp non idealities - Effect of Op-amp non idealities - finite gain bandwidth - Effect of ADC and DAC non idealities - Effect of Clock jitter.

Module:8	**Contemporary Issues**	**2 hours**
	Total Lecture hours:	**45 hours**

Text Book(s)

1. Frank Ohnhauser, Analog-Digital Converters for Industrial Applications Including an

	Introduction to Digital-Analog Converters, 2015, First Edition, Springer Publishers.		
2.	David Johns and Ken Martin, Analog Integrated Circuit Design, 2012, Second Edition John Wiley & Sons Inc.		
Reference Books			
1.	Ahmed M.A.Ali, High Speed Data Converters, 2016, First Edition, IET Materials, Circuits & Devices.		
2.	S.Pavan,R. Schreier and Gabor.C.Temes, Understanding Delta – Sigma Data Converters, 2017, First Edition , IEEE Press.		
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test			
Recommended by Board of Studies	28-07-2022		
Approved by Academic Council	No. 67	Date	08-08-2022

Course Code	Course Title	L	T	P	C
MVLD607L	RFIC Design	3	0	0	3
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives

The course is aimed to

1. Familiarize with the design of integrated radio frequency front-end circuits.
2. Design of transceivers.

Course Outcomes

At the end of the course the student will be able to

1. Understand the concepts of RF IC Design.
2. Understand the High Frequency model of MOS and importance of Impedance Matching.
3. Classify and comprehend the design of Power Amplifiers.
4. Design Low Noise amplifiers and Mixers with specifications.
5. Design VCOs and Frequency synthesizers and their applications to transceiver design.
6. Analyze and design of transceiver.

Module:1	**Introduction to RF & Wireless Technology:**	**5 hours**

Complexity design and applications - Choice of Technology - Basic concepts in RF Design: Nonlinearly - Time Variance - Intersymbol Interference - random processes - Noise. Definitions of sensitivity - dynamic range -conversion Gain and Distortion.

Module:2	**High Frequency Model of RF Transistors and Matching Networks:**	**5 hours**

MOSFET behavior at RF frequencies - Noise performance and limitation of devices - Impedance matching networks - transformers and baluns.

Module:3	**Low Noise Amplifiers and Mixers**	**5 hours**

Low Noise Amplifiers: Common Source LNA - Common Gate LNA -Cascode LNA. Mixers: Design of Active and Passive Mixers.

Module:4	**RF Power Amplifiers:**	**8 hours**

Class A, AB, B, C amplifiers - Class D, E, F amplifiers - RF Power amplifier design.

Module:5	**Voltage Controlled Oscillators:**	**8 hours**

Basic topologies, Types of Oscillator- Cross coupled Oscillator, Three-point Oscillator, LC VCOs architecture, Tuning range with continuous and discrete, VCO phase noise, Quadrature Oscillators- basic concepts and topologies.

Module:6	**Frequency Synthesizers:**	**8 hours**

Analysis of simple PLL, Charge-pump PLL, Jitter, Phase Noise, Frequency multiplication, Architectures-Integer-N and Fractional-N, Frequency divider.

Module:7	**Design of Transceiver:**	**4 hours**

System level specification, Receiver design, transmitter design, synthesizer design.

Module:8	**Contemporary Issues**	**2 hours**

Guest lectures from Industries and R&D Organizations

	Total Lecture hours:	**45 hours**

Text Book(s)

1. B.Razavi, RF Microelectronics, 2013, Second Edition, Pearson Education Limited.

2.	Hooman Darabi, Radio-Frequency Integrated Circuits and Systems, 2020, Second Edition Cambridge University Press, New York, USA.			
Reference Books				
1.	Gu, Qizheng, RF System Design of Transceivers for Wireless Communications, 2010, Springer, USA.			
2.	Bosco Leung, VLSI for Wireless Communication, 2011, Second Edition, Springer, USA.			
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test				
Recommended by Board of Studies		07-06-2023		
Approved by Academic Council		No. 70	Date	24-06-2023

Course Code	Course Title	L	T	P	C
MVLD608L	VLSI Digital Signal Processing	3	0	0	3
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives:

The course is aimed to

1. Familiarise various representation methods of DSP algorithms, understand the significance of the iteration bound and to calculate the same for a given single-rate and/or multi-rate DFG.
2. Understand and apply the architectural transformation techniques such as retiming, unfolding and folding on a given DFG.
3. Introduce the algorithmic and numerical strength reduction methods for performance improvement.
4. Signify and calculate the effects of scaling and round-off noise for a given digital filter with limited word length.

Course Outcomes:

At the end of the course the student will be able to

1. Compare various representation methods of DSP algorithms.
2. Find iteration bound of a given single and/or multi-rate DFG.
3. Understand and transform the given DFG using retiming with constraints.
4. Apply unfolding and folding transformations on the given DFG.
5. Understand and apply algorithmic and numerical strength reduction methods.
6. Understand and calculate scaling and round-off noise of the given digital filter with limited word length.

Module:1	**Introduction to Digital Signal Processing**	**5 hours**

Typical DSP Algorithms - DSP Application Demands and Scaled CMOS Technologies - Representations of DSP Algorithms - Data-Flow Graph Representations.

Module:2	**Iteration Bound**	**5 hours**

Introduction - Loop Bound and Iteration Bound - Algorithms for Computing Iteration Bound: Longest Path Matrix and Multiple Cycle Mean algorithms - Iteration Bound of Multi-rate Data Flow Graphs.

Module:3	**Pipelining, Parallel processing and Retiming**	**8 hours**

Pipelining and Parallel Processing - Introduction to Retiming - Definitions and Properties - Solving Systems of Inequalities - The Bellman-Ford Algorithm - The Floyd Warshall Algorithm- Retiming Techniques.

Module:4	**Unfolding**	**6 hours**

Introduction, An Algorithm for Unfolding, Properties of Unfolding, Critical Path, Unfolding, and Retiming, Applications of Unfolding.

Module:5	**Folding**	**6 hours**

Introduction, Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures.

Module:6	**Algorithmic & Numerical Strength Reduction**	**7 hours**

Introduction to Algorithmic Strength Reduction, Cook-Toom Algorithm, Iterated Convolution, Cyclic Convolution, Discrete Cosine Transform. Introduction to Numerical Strength Reduction, Canonic Signed Digit Arithmetic, Sub-expression Elimination, Multiple Constant Multiplication, Sub-expression Sharing in Digital Filters.

Module:7	**Scaling and Rounding Noise**	**6 hours**

Introduction, Scaling and Rounding Noise, State Variable Description of Digital Filters, Scaling and Rounding Noise Computation, Rounding Noise in Pipelined IIR Filters.

Module:8	**Contemporary Issues**	**2 hours**

	Total Lecture hours:	**45 hours**

Text Book(s)	
1.	Keshab. K.Parhi, VLSI Digital Signal Processing Systems: Design and Implementation, 2014, Reprint, Wiley.
Reference Books	
1.	John G. Proakis, Dimitris K Manolakis, Digital Signal Processing: Principles, Algorithms and Applications, 2015, Fourth Edition, Prentice Hall.
2.	Mohammed Ismail and Terri Fiez, Analog VLSI Signal and Information Processing, 2014, McGraw-Hill.
3.	S.Y. Kung, H.J. White House, T. Kailath, VLSI and Modern Signal Processing, 2010, PHI.
4.	S. K. Mitra, Digital Signal Processing – A Computer Based Approach, 2010, Fourth Edition, McGraw-Hill.

Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test			
Recommended by Board of Studies	28-07-2022		
Approved by Academic Council	No. 67	Date	08-08-2022

Course Code	Course Title	L	T	P	C
MVLD610L	Nanoscale Devices and Circuit Design	3	0	0	3
Pre-requisite	MVLD501L	Syllabus version			
		1.0			

Course Objectives:

The course is aimed to

1. Understand the CMOS scaling.
2. Design of digital, analog circuits using multigate devices, materials and their properties used for designing Microsensors.
3. Understand the concepts of Microsystem technologies used for realizing Microsensors and actuators.
4. Understand the working principles of Interface Electronic Circuits for resistive, capacitive and temperature sensors.

Course Outcomes:

At the end of the course the students will be able to

1. Understand the CMOS scaling issues
2. Explain the need of novel MOSFET
3. Explain the physics of multigate MOS system
4. Model nanowire FETs.
5. Design digital and analog circuit using multigate devices.
6. Understand the physics of CNTFET

Module:1	**CMOS Scaling Issues and Solutions**	**5 hours**
MOSFET scaling, short channel effects, quantum effects, volume inversion, threshold voltage, channel engineering, source/drain engineering, high-k dielectric, strain engineering, multigate technology mobility, gate stack.		
Module:2	**Introduction to Novel MOSFETs**	**4 hours**
SOI MOSFET, multigate transistors, single gate, double gate, triple gate, surround gate, Silicon Nanowire transistors		
Module:3	**Physics of Multi-gate MOS System**	**6 hours**
MOS electrostatics, 1D, 2D MOS electrostatics, ultimate limits, double gate MOS system, gate voltage effect, semiconductor thickness effect, asymmetry effect, oxide thickness effect , electron tunnel current, two dimensional confinement, scattering.		
Module:4	**Nanowire FETS**	**6 hours**
Silicon nanowire MOSFETs, evaluation of I-V characteristics, I-V characteristics for non-degenerate carrier statistics, I-V characteristics for degenerate carrier statistics, electronic conduction in molecules, general model for ballistic nano transistors, CNT-FETs.		
Module:5	**Digital Circuit Design using Multi-gate Devices**	**7 hours**
Digital circuits design, impact of device performance on digital circuits, leakage performance trade off, multi VT devices and circuits, SRAM design.		
Module:6	**Analog Circuit Design using Multi-gate Devices**	**9 hours**
Analog circuit design, trans-conductance, intrinsic gain, flicker noise, self-heating, band gap voltage reference, operational amplifier, comparator designs, mixed signal, successive approximation DAC, RF circuits		
Module:7	**Carbon Nanotube FET**	**6 hours**
CNT-FET, CNT memories, CNT based switches, logic gates, CNT based RF devices, CNT based RTDs, CNTFET based applications.		
Module:8	**Contemporary Issues**	**2 hours**
	Total Lecture hours:	**45 hours**

Text Book(s)

1. J P Colinge, FINFETs and other Multi-gate Transistors, 2010, Springer, Germany.

2.	B.G.Park, S.W. Hwang &Y.J.Park, Nanoelectronic Devices, 2012, Pan Stanford Publisher, Singapore.		
Reference Books			
1.	N. Collaert, CMOS Nanoelectronics: Innovative Devices, Architectures and Applications, 2012, Reprint Pan Stanford publisher, Singapore.		
2.	Niraj K. Jha, Deming Chen, Nanoelectronic Circuit Design, 2011, First Edition, Springer London.		
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test			
Recommended by Board of Studies	28-07-2022		
Approved by Academic Council	No. 67	Date	08-08-2022

Course Code	Course Title	L	T	P	C
MVLD611L	Advanced Computer Architecture	3	0	0	3
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives

The course is aimed to

1. Introduce advanced concepts of computer architecture.
2. Acquire knowledge on various interconnect topology for multiprocessor system and Different pipelining techniques.
3. Understanding different memory hierarchy for multiprocessor and multicomputer systems.

Course Outcomes

At the end of the course the student will be able to:

1. Understand the architecture of the various multiprocessors and multicomputer.
2. Determine the required static or dynamic interconnect network for a multiprocessor system.
3. Understand the Data level parallelism in Vector architecture, SIMD, GPU
4. Apply different pipelining techniques to reduce computation time.
5. Analyse the various memory design for multiprocessor and multicomputer.
6. Design scalable parallel architecture for multiprocessor system.

Module:1	Parallel computer models	5 hours

The state of computing - Conditions of parallelism - Data and resource Dependences - Hardware and software parallelism - Program partitioning and scheduling - Grain Size and latency Classification of parallel computers - Multiprocessors and Multicomputer

Module:2	System Interconnect Architectures	7 hours

Network properties and routing - Static interconnection Networks - Dynamic interconnection Networks - Multiprocessor system Interconnects - Hierarchical bus systems - Crossbar switch and multiport memory - Multistage and combining network.

Module:3	Data level Parallelism in Vector and GPU Architectures	7 hours

Vector Architecture- RISC-V Vector extension- Vector computation instructions, Registers and dynamic typing, loads and store, parallelism during vector execution, SIMD Instruction extension for multimedia-Graphics Processing Units- Detecting and enhancing loop-level parallelism

Module:4	Pipelining	7 hours

Linear pipeline processor - nonlinear pipeline processor - Instruction pipeline Design - Mechanisms for instruction pipelining - Dynamic instruction scheduling - Branch Handling techniques - branch prediction - Arithmetic Pipeline Design.

Module:5	Memory Hierarchy Design	6 hours

Cache basics & cache performance - reducing miss rate and miss penalty - multilevel cache hierarchies - main memory organizations - design of memory hierarchies.

Module:6	Shared Memory Architectures	6 hours

Symmetric shared memory architectures – distributed shared memory architectures – cache coherence protocols – scalable cache coherence – directory protocols – memory-based directory protocols – cache-based directory protocols.		
Module:7	**Multiprocessor Architectures**	**5 hours**
Computational models – An Argument for parallel Architectures – Scalability of Parallel Architectures – Benchmark Performances.		
Module:8	**Contemporary Issues**	**2 hours**
Guest lectures from Industries and R & D Organizations		
	Total Lecture hours:	**45 hours**

Text Book(s)	
1.	Kai Hwang, NareshJotwani, Advanced Computer Architecture: Parallelism, Scalability, Programmability, 2017, Third edition, Tata McGraw Hill Education, India.
2.	David Patterson, Andrew Waterman, The RISC-V Reader: An Open Architecture Atlas, 2017, First edition, Strawberry Canyon, USA.
Reference Books	
1.	John L. Hennessy, David A. Patterson, Computer Architecture: A Quantitative Approach, 2011, Fifth edition, Morgan Kaufmann.
2.	DezsoSima, Terence Fountain, Peterr Karsuk, Advanced computer Architectures – A Design Space Approach, 2014, Pearson Education, India.
3.	Ananth Grama, Anshul Gupta, George Karypis and Vipin Kumar, —Introduction to Parallel Computing, 2009, Second edition, Pearson Education, India.
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test.	

Recommended by Board of Studies	07-06-2023		
Approved by Academic Council	No. 70	Date	24-06-2023

Course Code	Course Title	L	T	P	C
MVLD613L	System Design with FPGA	3	0	0	3
Prerequisite	NIL	Syllabus version			
		1.0			

Course Objectives :

This course is aimed to

1. Provide an overview of FPGA architectures and expound on the softcore and hard- core processors in association with hardware and software co-design.
2. Understand the specification and operation of Programming for peripheral Interfaces and Interconnect Fabrics.
3. Implement digital system and IP blocks for various DSP algorithms.

Course Outcomes :

After completion of the course the student will be able to:

1. Understand and get an idea about SoC and FPGA architectures.
2. Understand the NIOS II soft core processor architecture.
3. Analyze the working of hardware and software co-design flow.
4. Interpret the usage of various peripheral interfaces for system design.
5. Develop a system by choosing suitable interconnect fabrics.
6. Design the system using NIOS II soft core processor, model the system by using IP block and design and develop embedded synthesis using FPGA.

Module:1	**SoC Architecture**	**6 hours**
An Overview of System on Design – FPGA SoC Architecture – Case Study: Xilinx / Intel FPGA		
Module:2	**Soft Core and Hard Core Processor**	**10 hours**
Processor Architecture and Configurability Features: Nios II Processor – Nios V Processor – ARM cortex A9 architecture		
Module:3	**Hardware – Software Co-design Flow**	**2 hours**
Hardware Design Flow – Software Design Flow - EDA Tool Hardware and Software design flow		
Module:4	**Programming for peripheral Interfaces**	**5 hours**
LCD, PS2, RS232, SDRAM, SRAM Controller, VGA, Audio and Video, PIO, External Bus bridge, and IrDA		
Module:5	**Interconnect Fabrics**	**4 hours**
Avalon Switch Fabric Interconnect - Implementation and Functions-Integrated Design Environment		
Module:6	**System Design**	**8 hours**
Traffic light Controller, Real Time Clock - Interfacing using FPGA: VGA, LCD, Camera		
Module:7	**IP cores based SoC design**	**8 hours**
Edge detection algorithm- Image edge detection in FPGA using SOBEL Edge Detection/ Canny Edge Detection Algorithm, Colour and Brightness Enhancement algorithm- Contrast enhancement using RGB to HSV algorithm based on FPGA – SRAM Configuration using Controllers		
Module:8	**Contemporary Issues**	**2 hours**
Guest lecture from Industry and R & D Organizations		
	Total Lecture hours:	**45 hours**

Text Book(s)

1.	ZainalabedinNavabi, "Embedded Core Design with FPGAs", 2011, Tata McGraw Hill Ltd, India.
2.	Pong P. Chu, Embedded SoPC Design with NIOS II Processor and VERILOG examples", 2012, Wiley, USA.
Reference Books	
1	Donald G. Bailey," Design for Embedded Image Processing on FPGAs", 2012, Wiley, USA.
2	Jivan S. Parab, Rajendra S Gad, G.M. Naik, "Hands-on Experience with Altera FPGA Development Boards", 2018, Springer, USA.
3	Joseph Yu, System-on-Chip Design with Arm Cortex-M Processors, 2019, ARM Education Media
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test.	
Recommended by Board of Studies	07-06-2023
Approved by Academic Council	No. 70 Date 24-06-2023

Course Code	Course Title	L	T	P	C
MVLD616L	Scripting Languages For Electronic Design Automation	3	0	0	3
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives:

The course is aimed to

1. To write scripts in the LINUX environment.
2. To study the principles of Scripting Languages like Perl, TCL and Python.
3. To write the scripts for automation using the languages like Perl, TCL and Python.

Course Outcomes:

At the end of the course the student will be able to

1. Explain and apply commands in LINUX environment.
2. Develop and execute the Perl scripts.
3. Analyze and Handle files, directories and manage processes using Perl scripts.
4. Use TCL scripts for automation.
5. Build TCL scripts to Handle files, directories and manage process.
6. Develop Python scripts to interpret files and directories.

Module:1	**LINUX Basics**	**5 hours**
Introduction to Linux, File System of Linux, General usage of Linux Kernel and Basic Commands, Linux users and group, Permissions for file, directory and users, Searching a file and directory, zipping and unzipping concepts.		
Module:2	**PERL Basics**	**7 hours**
History and Concepts of PERL - Scalar Data - Arrays and List Data - Control structures – Hashes - Basics I/O - Regular Expressions – Functions - Miscellaneous control structures - Formats.		
Module:3	**Advanced Topics in PERL**	**6 hours**
Directory access - File and Directory manipulation - Process Management - Packages and Modules -Applications of PERL scripts to Electronic Design Automation.		
Module:4	**TCL Basics**	**7 hours**
An Overview of TCL and Tk -Tcl Language syntax – Variables – Expressions – Lists - Control flow – procedures - Errors and exceptions - String manipulations.		
Module:5	**Advanced Topics in TCL**	**6 hours**
Accessing files- Processes. Applications - Controlling Tools - Basics of Tk.		
Module:6	**Python Basics**	**6 hours**
Introduction to Python – Using Python interpreter – Brief tour on standard library - Control flow Tools – Data structures – Regular Expressions.		
Module:7	**Advanced Topics in Python**	**6 hours**
Input and Output – Errors and Exceptions – Classes – Modules- Applications of Python scripts to Electronic Design Automation.		
Module:8	**Contemporary Issues:**	**2 hours**
Guest lectures from Industry and R&D Organizations		
	Total Lecture hours:	**45 hours**

Text Book(s)				
1.	Larry Wall, Tom Christiansen, John Orwant, Programming PERL, 2012, Fourth Edition, Oreilly Publications.			
2.	John K. Ousterhout, Ken Jones, Tcl and the Tk Toolkit, 2010, Second Edition, Pearson Education, India			
Reference Books				
1.	Guido van Rossum Fred L. Drake, Jr., editor, Python Tutorial Release 3.2.3, 2012, Python Software Foundation.			
2.	Randal L. Schwartz, Brian D Foy, Tom Phoenix, Learning Perl, 2021, 8th Edition, O'Reilly Media, Inc.			
3.	Mark Lutz, Learning Python, 2013, 5th Edition, O'Reilly Media, Inc.			
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test				
Recommended by Board of Studies		07-06-2023		
Approved by Academic Council		No. 70	Date	24-06-2023

Course Code	Course Title	L	T	P	C
MVLD617L	Neuromorphic Engineering and Hardware Accelerators	3	0	0	3
Pre-requisite	NIL	Syllabus Version			
		1.0			

Course Objectives:

The course is aimed to

1. Provide an overview of the current trends and methods in Neuromorphic Engineering.
2. Describe the neuronal dynamics of biological neural circuits.
3. Describe the mechanisms of signal encoding, plasticity, and network.
4. To design a system with multiple supply and threshold voltages applicable for various applications.
5. Discuss the fundamental concepts and current trends in designing neuromorphic devices, circuits and systems.

Course Outcomes:

At the end of the course the student will be able to:

1. Understand various aspects of computational neuroscience.
2. Demonstrate the trade-offs between various neuromorphic implementations.
3. Demonstrate the ability to identify and formulate problems of neuromorphic computing.
4. Perform analog electrical modelling of Neuromorphic Blocks.
5. Utilize computer design tools and experimental measurement in the design of neuromorphic Architectures.
6. Understanding Neuromorphic Accelerators

Module:1	Brain as a potential Technology	4 hours

The Nature of Neuronal Computation, Approaches to Understanding Brains, An Example Model of Neural Circuit Processing, Toward Neuromorphic Cognition.

Module:2	Artificial Neural Networks in Hardware	6 hours

Digital Accelerators, FPGA-Based Accelerators, Analog/Mixed-Signal Accelerators, Case Study: An Energy-Efficient Accelerator for Adaptive Dynamic Programming.

Module:3	Hardware implementation of Spiking Neural Networks	7 hours

Different Generations of Neural Networks, Spiking Neuron Operating Principle, Models of Spiking Neurons, Methods of Data Representation in Spiking Neural Networks and Network Learning Methods, Assessment of Network Processing Efficiency. Edge Computing Using Spiking Neurons, Hardware Aspects of Semiconductor Implementations of Spiking Neurons, Network Reconfiguration, Synapse Plasticity, Neuro-Processors.

Module:4	Understanding Neuromorphic System	7 hours

Address-Event Representation, AER Encoders, Arbitration Mechanisms, Encoding Mechanisms, Multiple AER Endpoints, Address Mapping, Routing, Considerations for AER Link Design.

Module:5	Building Neuromorphic Systems- Silicon Neurons	6 hours

Introduction, Silicon Neuron Circuit Blocks, Conductance Dynamics Spike-Event Generation, Spiking Thresholds and Refractory Periods, Spike-Frequency Adaptation and Adaptive Thresholds, Axons and Dendritic Trees, Additional Useful Building Blocks, Silicon Neuron Implementations, Subthreshold Biophysically Realistic Models, Compact I&F Circuits for Event-Based Systems, Generalized I&F Neuron Circuits, Above Threshold, Accelerated-Time, and Switched-Capacitor Designs.		
Module:6	**Building Neuromorphic Systems- Silicon Synapse**	**8 hours**
Introduction, Silicon Synapse Implementations, Non-Conductance-Based Circuits Conductance-Based Circuits, NMDA Synapse, Dynamic Plastic Synapses, Short-Term Plasticity, Long-Term Plasticity.		
Module:7	**Accelerating DNNs in Hardware**	**5 hours**
GPUs, Spatial Accelerators, Systolic Arrays, HW-SW Co-Design, Binary Neural Networks, Bit-Precision, Pruning and Sparsity, Vector Architectures, FPGAs and GPU Architectures, ASIC Accelerators, In-Memory Computing Accelerator Design, Neuromorphic Accelerators, Custom and reconfigurable accelerators, Case studies on architectures for machine learning, Emerging Technologies, ReRAM, Analog Accelerators, Emerging Hardware Architectures, Memristor based designs, Spiking Architectures.		
Module:8	**Contemporary Issues**	**2 hours**
Guest lecture from Industry and R & D Organizations		
	Total Lecture hours:	**45 hours**
Text Book(s)		
1.	Liu, Shih-Chii, Tobi Delbruck, Giacomo Indiveri, Adrian Whatley, and Rodney Douglas, Event-based neuromorphic systems, 2014, John Wiley & Sons, USA.	
2.	Gerstner, Wulfram, Werner M. Kistler, Richard Naud, and Liam Paninski. Neuronal dynamics: From Single Neurons to Networks and Models of Cognition, 2014, Cambridge University Press, USA.	
Reference Books		
1.	Amari, Shun'ichi. The Handbook of Brain Theory and Neural Networks, 2003, MIT press, Cambridge, USA.	
2.	Mead, Carver, and Mohammed Ismail, Analog VLSI Implementation of Neural Systems, 1989, Springer Science & Business Media, USA.	
3.	Jan M.Rabaey, Massoud Pedram, Low power Design methodologies, 2014, First Edition, Springer, US.	
4.	Abderazek Ben Abdallah and Khanh Dang Ngo Neuromorphic Computing Principles and Organization, 2022, First Edition, Springer, USA.	
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test.		
Recommended by Board of Studies	07-06-2023	
Approved by Academic Council	No. 70	Date 24-06-2023

Course Code	Course Title	L	T	P	C
MEDS601L	Electromagnetic Interference and Compatibility	3	0	0	3
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives

The course is aimed at:

1. Imparting knowledge about EMI environment
2. Teaching EMI coupling principles, EMI control techniques and design of PCBs for EMC
3. Giving exposure to EMI Standards, Regulations and Measurements

Course Outcomes

At the end of the course, the student will be able to

1. Understand terminologies of EMI and EMC
2. Analyze and understand various EMI coupling mechanisms
3. List various EMI Test and Measurement methods
4. Analyze various techniques needed to suppress EMI
5. Perceive different EMC regulations followed worldwide
6. Ability to design an Electromagnetic Compatible systems.
7. Analyze and comprehend different techniques needed for Signal Integrity and ability to understand various models for EMI/EMC

Module:1	EMI Environment	4 hours

EMI-EMC Definitions and units of Parameters, Sources of EMI, conducted and radiated EMI, Transient EMI

Module:2	EMI Coupling Mechanisms	6 hours

Conducted, Radiated and Transient Coupling, Common Impedance Ground Coupling, Radiated Common Mode and Ground Loop Coupling, Radiated Differential Mode Coupling, Near Field Cable to Cable Coupling, Power Mains and Power Supply Coupling.

Module:3	EMI Test and Measurements	8 hours

EMI Specification / Standards / Limits: Units of specifications, Civilian standards Military standards. EMI Test Instruments / Systems, EMI Test, EMI Shielded Chamber, Open Area Test Site, TEM Cell Antennas, Conductors Sensors/Injectors/Couplers. EMI Measurement Methods: Military Test Method and Procedures, Calibration Procedures, Modeling interferences

Module:4	EMI Control Techniques	7 hours

Shielding, Filtering, Grounding, Bonding, Isolation Transformer, Transient Suppressors, Cable Routing, Signal Control, Component Selection and Mounting, Electrostatic discharge protection schemes

Module:5	EMC Standards and Regulations	5 hours

National and Intentional standardizing organizations- FCC, CISPR, ANSI, DOD, IEC, CENEEC, FCC CE and RE standards, CISPR, CE and RE Standards, IEC/EN, CS standards, SAE Automotive EMC standard, Frequency assignment - spectrum conversation.

Module:6	System Design for EMC	8 hours

PCB Traces Cross Talk, Impedance Control, Power Distribution Decoupling, Zoning, Motherboard Designs and Propagation Delay Performance Models,

System Enclosures, Power line filter placement, Interconnection and Number of Printed Circuit Boards, PCB and subsystem decoupling		
Module:7	**Signal Integrity and EMI/EMC Models**	**5 hours**
Effect of terminations on line wave forms, Matching schemes for Signal Integrity, Effects of line discontinuities, Statistical EMI/EMC models.		
Module:8	**Contemporary Issues**	**2 hours**
Guest Lectures from Industry and, Research and Development Organizations		
	Total Lecture hours:	**30 hours**
Text Book(s)		
1.	Clayton R. Paul,IntroductiontoElectromagneticcompatibility,2010, 2nd edition., Wiley & Sons, New Jersey	
Reference Books		
1.	HenryW.ott, Electromagnetic Compatibility Engineering, 2011, 1sted. John Wiley and Sons, NewJersey.	
2.	Patrick G. André and Kenneth Wyatt, EMI Troubleshooting Cookbook for Product Designers 2014, 1st ed., SciTech Publishing, New Jersey	
Mode of Evaluation: Continuous Assessment, Digital Assignment, Quiz and Final Assessment Test		
Recommended by Board of Studies	07-06-2023	
Approved by Academic Council	No. 70	Date 24-06-2023

Course Code	Course Title	L	T	P	C
MEDS616L	Machine Leaning and Deep Learning	3	0	0	3
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives

The course is aimed at

1. Understanding about the fundamentals of machine learning and neural networks
2. Enabling the students to acquire knowledge about pattern recognition.
3. Motivating the students to apply deep learning algorithms for solving real life problems.

Course Outcomes

At the end of the course the student will be able to

1. Comprehend the categorization of machine learning algorithms.
2. Understand the types of neural network architectures, activation functions
3. Acquaint with the pattern association using neural networks
4. Explore various terminologies related with pattern recognition
5. Adopt different feature selection and classification techniques
6. Understand the architectures of convolutional neural networks and Comprehend advanced neural network architectures such as RNN, Autoencoders, and GANs.

Module:1	Learning Problems and Algorithms	4 hours

Various paradigms of learning problems, Supervised, Semi-supervised and Unsupervised algorithms

Module:2	Neural Network – I	8 hours

Differences between Biological and Artificial Neural Networks - Typical Architecture, Common Activation Functions, Multi-layer neural network, Linear Separability, Hebb Net, Perceptron, Adaline, Standard Back propagation

Module:3	Neural Network – II	8 hours

Training Algorithms for Pattern Association - Hebb rule and Delta rule, Hetero associative, Auto associative, Kohonen Self Organising Maps, Examples of Feature Maps, Learning Vector Quantization, Gradient descent, Boltzmann Machine Learning

Module:4	Machine Learning: Terminologies	7 hours

Classifying Samples: The confusion matrix, Accuracy, Precision, Recall, F1- Score, the curse of dimensionality, training, testing, validation, cross validation, overfitting, under-fitting the data, early stopping, regularization, bias and variance

Module:5	Machine Learning: Feature Selection and Classification	7 hours

Feature Selection, normalization, dimensionality reduction, Classifiers: KNN, SVM, Decision trees, Naïve Bayes, Binary classification, multi class classification, clustering.

Module:6	Convolutional Neural Networks	5 hours

Feed forward networks, Activation functions, backpropagation in CNN, optimizers, batch normalization, convolution layers, pooling layers, fully connected layers, dropout, Examples of CNNs.

Module:7	**RNNs, Auto encoders and GANs**	**4 hours**
State, Structure of RNN Cell, LSTM and GRU, Time distributed layers, Generating Text, Auto encoders: Convolutional Auto encoders, De-noising auto encoders, Variational auto encoders, GANs: The discriminator, generator, DCGANs		
Module:8	**Contemporary Issues**	**2 hours**
Guest Lectures from Industry and, Research and Development Organizations		
	Total Lecture hours:	**45 hours**
Text Book(s)		
1.	J. S. R. Jang, C. T. Sun, E. Mizutani, Neuro Fuzzy and Soft Computing - A Computational Approach to Learning and Machine Intelligence, 2012, PHI learning	
2.	Deep Learning, Ian Good fellow, Yoshua Bengio and Aaron Courville, MIT Press, ISBN: 9780262035613, 2016.	
Reference Books		
1.	The Elements of Statistical Learning. Trevor Hastie, Robert Tibshirani and Jerome Friedman. Second Edition. 2009.	
2.	Understanding Machine Learning. ShaiShalev-Shwartz and Shai Ben-David. Cambridge University Press. 2017.	
Mode of Evaluation: Continuous Assessment, Digital Assignment, Quiz and Final Assessment Test		
Recommended by Board of Studies	07-06-2023	
Approved by Academic Council	No. 70	Date 24-06-2023

Course Code	Course Title	L	T	P	C
MEDS501L	Embedded System Design	3	0	0	3
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives

The course aimed at

1. Ability to understand comprehensively the technologies and techniques underlying in building an embedded solution to a wearable, mobile and portable system.
2. Analyze UML diagrams and advanced Modelling schemes for different use cases.
3. Understand the building process of embedded systems

Course Outcome

The students will be able to

1. Define an embedded system and compare with general purpose system.
2. Appreciate the methods adapted for the development of a typical embedded system.
3. Get introduced to RTOS and related mechanisms.
4. Classify types of processors and memory architecture
5. Differentiate the features of components and networks in embedded systems
6. Develop real-time working prototypes of different small-scale and medium-scale embedded Systems.
7. Apprehend the various concepts in Multi-Tasking

Module:1	**Introduction to Embedded System**	**5 hours**
Embedded system processor, hardware unit, software embedded into a system, Example of an embedded system, Embedded Design life cycle, Layers of Embedded Systems.		
Module:2	**Embedded System Design Methodologies**	**5 hours**
Embedded System modelling [FSM, SysML, MARTE], UML as Design tool, UML notation, Requirement Analysis and Use case Modelling, Design Examples		
Module:3	**Building Process For Embedded Systems**	**4 hours**
Preprocessing, Compiling, Cross Compiling, Linking, Locating, Compiler Driver, Linker Map Files, Linker Scripts and scatter loading, Loading on the target, Embedded File System.		
Module:4	**System design using general purpose processor**	**7 hours**
Microcontroller architectures (RISC, CISC), Embedded Memory, Strategic selection of processor and memory, Memory Devices and their Characteristics, Cache Memory and Various mapping techniques, DMA.		
Module:5	**Component Interfacing & Networks**	**9 hours**
Memory Interfacing, I/O Device Interfacing, Interrupt Controllers, Networks for Embedded systems- USB, PCI,PCI Express, UART, SPI, I2C, CAN, Wireless Applications - Bluetooth, Zigbee,Wi-Fi.,6LoWPAN , Evolution of Internet of things (IoT).		
Module:6	**Operating Systems**	**7 hours**
Introduction to Operating Systems, Basic Features & Functions of an Operating System, Kernel & its Features [polled loop system, interrupt driven system, multi rate system], Processes/Task and its states, Process/Task Control Block, Threads, Scheduler, Dispatcher.		
Module:7	**Multi Tasking**	**6 hours**
Context Switching , Scheduling and various Scheduling algorithms, Inter-process Communication (Shared Memory, Mail Box, Message Queue), Inter Task Synchronization (Semaphore, Mutex), Dead Lock, Priority Inversion (bounded and unbounded), Priority Ceiling Protocol & Priority Inheritance Protocol		
Module:8	**Contemporary Issues**	**2 hours**
	Total Lecture hours:	**45 hours**

Text Book(s)			
1.	Raj Kamal, “Embedded systems Architecture, Programming and Design”, Tata McGraw- Hill, 2016.		
2.	Wayne Wolf “Computers as components: Principles of Embedded Computing System Design”, The Morgan Kaufmann Series in Computer Architecture and Design, 2013.		
Reference Books			
1.	Lyla B. Das," Embedded Systems an Integrated Approach", Pearson Education, 2013.		
2.	Shibu K V," Introduction to Embedded Systems", McGraw Hill Education(India) Private Limited, 2014		
3.	Sriram V Iyer, Pankaj Gupta " Embedded Real Time Systems Programming", Tata McGraw- Hill, 2012		
4.	Steve Heath, “Embedded Systems Design”, EDN Series, 2013.		
Mode of Evaluation: Continuous Assessment, Digital Assignment, Quiz and Final Assessment Test			
Recommended by Board of Studies	28-07-2022		
Approved by Academic Council	No. 67	Date	08-08-2022

Course Code	Course Title	L	T	P	C
MVLD696J	Study Oriented Project				02
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives:

1. The student will be able to analyse and interpret published literature for information pertaining to niche areas.
2. Scrutinize technical literature and arrive at conclusions.
3. Use insight and creativity for a better understanding of the domain of interest.

Course Outcome:

1. Retrieve, analyse, and interpret published literature/books providing information related to niche areas/focused domains.
2. Examine technical literature, resolve ambiguity, and develop conclusions.
3. Synthesize knowledge and use insight and creativity to better understand the domain of interest.
4. Publish the findings in the peer reviewed journals / National / International Conferences.

Module Content	(Project duration: One semester)

This is oriented towards reading published literature or books related to niche areas or focussed domains under the guidance of a faculty.

Mode of Evaluation: Evaluation involves periodic reviews by the faculty with whom the student has registered. Assessment on the project – Report to be submitted, presentation and project reviews – Presentation in the National / International Conference on Science, Engineering Technology.

Recommended by Board of Studies	28-07-2022		
Approved by Academic Council	No. 67	Date	08-08-2022

Course Code	Course Title	L	T	P	C
MVLD697J	Design Project				02
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives:

1. Students will be able to design a prototype or process or experiments.
2. Describe and demonstrate the techniques and skills necessary for the project.
3. Acquire knowledge and better understanding of design systems.

Course Outcome:

1. Develop new skills and demonstrate the ability to upgrade a prototype to a design prototype or working model or process or experiments.
2. Utilize the techniques, skills, and modern tools necessary for the project.
3. Synthesize knowledge and use insight and creativity to better understand and improve design systems.
4. Publish the findings in the peer reviewed journals / National / International Conferences.

Module Content	(Project duration: One semester)

Students are expected to develop new skills and demonstrate the ability to develop prototypes to design prototype or working models related to an engineering product or a process.

Mode of Evaluation: Evaluation involves periodic reviews by the faculty with whom the student has registered. Assessment on the project – Report to be submitted, presentation and project reviews – Presentation in the National / International Conference on Science, Engineering Technology.

Recommended by Board of Studies	28-07-2022		
Approved by Academic Council	No. 67	Date	08-08-2022

Course Code	Course Title	L	T	P	C
MVLD698J	Internship I/ Dissertation I				10
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives:

To provide sufficient hands-on learning experience related to the design, development and analysis of suitable product / process so as to enhance the technical skill sets in the chosen field and also to give research orientation.

Course Outcome:

1. Considerably more in-depth knowledge of the major subject/field of study, including deeper insight into current research and development work.
2. The capability to use a holistic view to critically, independently and creatively identify, formulate and deal with complex issues.
3. A consciousness of the ethical aspects of research and development work.
4. Publications in the peer reviewed journals / International Conferences will be an added advantage.

Module Content	(Project duration: one semester)

1. Dissertation may be a theoretical analysis, modeling & simulation, experimentation & analysis, prototype design, fabrication of new equipment, correlation and analysis of data, software development, applied research and any other related activities.
2. Dissertation should be individual work.
3. Carried out inside or outside the university, in any relevant industry or research institution.
4. Publications in the peer reviewed journals / International Conferences will be an added advantage.

Mode of Evaluation: Assessment on the project - Dissertation report to be submitted, presentation, project reviews and Final Oral Viva Examination.

Recommended by Board of Studies	28-07-2022		
Approved by Academic Council	No. 67	Date	08-08-2022

Course Code	Course Title	L	T	P	C
MVLD699J	Internship II/ Dissertation II				12
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives:

To provide sufficient hands-on learning experience related to the design, development and analysis of suitable product / process so as to enhance the technical skill sets in the chosen field.

Course Outcome:

Upon successful completion of this course students will be able to

1. Formulate specific problem statements for ill-defined real life problems with reasonable assumptions and constraints.
2. Perform literature search and / or patent search in the area of interest.
3. Conduct experiments / Design and Analysis / solution iterations and document the results.
4. Perform error analysis / benchmarking / costing.
5. Synthesize the results and arrive at scientific conclusions / products / solution.
6. Document the results in the form of technical report / presentation.

Module Content **(Project duration: one semester)**

1. Dissertation may be a theoretical analysis, modeling & simulation, experimentation & analysis, prototype design, fabrication of new equipment, correlation and analysis of data, software development, applied research and any other related activities.
2. Dissertation should be individual work.
3. Carried out inside or outside the university, in any relevant industry or research institution.
4. Publications in the peer reviewed journals / International Conferences will be an added advantage.

Mode of Evaluation: Assessment on the project - Dissertation report to be submitted, presentation, project reviews and Final Oral Viva Examination.

Recommended by Board of Studies	28-07-2022		
Approved by Academic Council	No. 67	Date	08-08-2022

Course code	Course Title	L	T	P	C
MENG501P	Technical Report Writing	0	0	4	2
Pre-requisite	Nil	Syllabus version			
		1.0			

Course Objectives

1.To develop writing skills for preparing technical reports.
2. To analyze and evaluate general and complex technical information.
3. To enable proficiency in drafting and presenting reports.

Course Outcome

At the end of the course, the student will be able to
1.Construct error free sentences using appropriate grammar, vocabulary and style.
2. Apply the advanced rules of grammar for proofreading reports.
3. Interpret information and concepts in preparing reports.
4. Demonstrate the structure and function of technical reports.
5. Improve the ability of presenting technical reports.

Indicative Experiments	
1.	**Basics of Technical Communication** General and Technical communication, Process of communication, Levels of communication
2.	**Vocabulary& Editing** Word usage: confusing words, Phrasal verbs Punctuation and Proof reading
3.	**Advanced Grammar** Shifts: Voice, Tense, Person, Number Clarity: Pronoun reference, Misplace and unclear modifiers
4.	**Elements of Technical writing** Developing paragraphs, Eliminating unnecessary words, Avoiding clichés and slang Sentence clarity and combining
5.	**The Art of condensation** Steps to effective precis writing, Paraphrasing and summarizing
6.	**Technical Reports:** Meaning, Objectives, Characteristics and Categories
7.	**Formats of reports and Prewriting**: purpose, audience, sources of information, organizing the material
8.	**Data Visualization** Interpreting Data - Graphs - Tables – Charts - Imagery - Info graphics
9.	**Systematization of Information:** Preparing Questionnaire Techniques to Converge Objective-Oriented data in Diverse Technical Reports
10.	**Research and Analyses:** Writing introduction and literature review, Reference styles, Synchronize Technical Details from Magazines, Articles and e-content
11..	**Structure of Reports** Title – Preface – Acknowledgement - Abstract/Summary – Introduction - Materials and Methods – Results – Discussion - Conclusion - Suggestions/Recommendations
12.	**Writing the Report:** First draft, Revising, Thesis statement, Developing unity and coherence
13.	**Writing scientific abstracts:** Parts of the abstract, Revising the abstract Avoiding Plagiarism, Best practices for writers
14.	**Supplementary Texts** Appendix – Index – Glossary – References – Bibliography - Notes
15	**Presentation**

	Presenting Technical Reports Planning, creating anddigital presentation of reports			
			Total Laboratory hours :	**60 hours**
Text Book(s)				
1.	Raman, Meenakshi and Sangeeta Sharma, (2015).Technical Communication: Principles and Practice, Third edition, Oxford University Press, New Delhi.			
Reference Books				
1.	Aruna, Koneru, (2020). English Language Skills for Engineers. McGraw Hill Education, Noida.			
2.	Rizvi,M. Ashraf (2018)Effective Technical Communication Second Edition. McGraw Hill Education, Chennai.			
3.	Kumar, Sanjay and Pushpalatha, (2018). English Language and Communication Skills for Engineers, Oxford University Press.			
4.	Elizabeth Tebeaux and Sam Dragga, (2020).The Essentials of Technical Communication, Fifth Edition, Oxford University Press.			
Mode of Evaluation **:** Continuous Assessment Tests, Quizzes, Assignment, Final Assessment Test				
Recommended by Board of Studies	19-05-2022			
Approved by Academic Council	No. 66	Date	16-06-2022	

Course Code	Course Title	L	T	P	C
MSTS501P	Qualitative Skills Practice	0	0	3	1.5
Pre-requisite	Nil	Syllabus version			
		1.0			

Course Objectives:

1. To develop the quantitative ability for solving basic level problems.
2. To improve the verbal and professional communication skills.

Course Outcome:

At the end of the course, the student will be able to

1. Execute appropriate analytical skills.
2. Solve problems pertaining to quantitative and reasoning ability.
3. Learn better vocabulary for workplace communication.
4. Demonstrate appropriate behavior in an organized environment.

Module:1	**Business Etiquette: Social and Cultural Etiquette; Writing Company Blogs; Internal Communications and Planning: Writing press release and meeting notes**	**9 hours**

Value, Manners- Netiquette, Customs, Language, Tradition, Building a blog, Developing brand message, FAQs', Assessing Competition, Open and objective Communication, Two way dialogue, Understanding the audience, Identifying, Gathering Information,. Analysis, Determining, Selecting plan, Progress check, Types of planning, Write a short, catchy headline, Get to the Point –summarize your subject in the first paragraph., Body– Make it relevant to your audience.

Module:2	**Time management skills**	**3 hours**

Prioritization, Procrastination, Scheduling, Multitasking, Monitoring, Working under pressure and adhering to deadlines

Module:3	**Presentation skills – Preparing presentation; Organizing materials; Maintaining and preparing visual aids; Dealing with questions**	**7 hours**

10 Tips to prepare PowerPoint presentation, Outlining the content, Passing the Elevator Test, Blue sky thinking, Introduction , body and conclusion, Use of Font, Use of Color, Strategic presentation, Importance and types of visual aids, Animation to captivate your audience, Design of posters, Setting out the ground rules, Dealing with interruptions, Staying in control of the questions, Handling difficult questions.

Module:4	**QuantitativeAbility-L1–Numberproperties; Averages; Progressions; Percentages; Ratios**	**11 hours**

Number of factors, Factorials, Remainder Theorem, Unit digit position, Tens digit position, Averages, Weighted Average, Arithmetic Progression, Geometric Progression, Harmonic Progression, increase and Decrease or Successive increase, Types of ratios and proportions.

Module:5	**Reasoning Ability - L1 – Analytical Reasoning**	**8 hours**

Data Arrangement (Linear and circular & Cross Variable Relationship), Blood Relations, Ordering / ranking / grouping, Puzzle test, Selection Decision table.

Module:6	**Verbal Ability -L1 – Vocabulary Building**	**7 hours**

Synonyms & Antonyms, One word substitutes, Word Pairs, Spellings, Idioms, Sentence completion, Analogies.		
	Total Lecture hours:	**45 hours**
Reference Books		
1.	Kerry Patterson, Joseph Grenny, Ron McMillan and Al Switzler, (2017).2nd Edition, Crucial Conversations: Tools for Talking when Stakesare High .McGraw-Hill Contemporary, Bangalore.	
2.	Dale Carnegie,(2016).How to Win Friends and Influence People. Gallery Books, New York.	
3.	Scott Peck. M, (2003). Road Less Travelled. Bantam Press, New York City.	
4.	SMART, (2018). Place Mentor, 1st edition. Oxford University Press, Chennai.	
5.	FACE, (2016). Aptipedia Aptitude Encyclopedia. Wiley publications, Delhi.	
6.	ETHNUS, (2013). Aptimithra. McGraw – Hill Education Pvt .Ltd, Bangalore.	
Websites:		
1.	**www.chalkstreet.com**	
2.	**www.skillsyouneed.com**	
3.	**www.mindtools.com**	
4.	**www.thebalance.com**	
5.	**www.eguru.ooo**	
Mode of Evaluation: Continuous Assessment Tests, Quizzes, Assignment, Final Assessment Test		
Recommended by Board of Studies	19-05-2022	
Approved by Academic Council	No.66	Date 16-06-2022

Course Code	Course Title	L	T	P	C
MSTS502P	Quantitative Skills Practice	0	0	3	1.5
Pre-requisite	Nil	Syllabus version			
		1.0			

Course Objectives:

1. To develop the students' advanced problem solving skills.
2. To enhance critical thinking and innovative skills.

Course Outcome:

At the end of the course, the student will be able to

1. Create positive impression during official conversations and interviews.
2. Demonstrate comprehending skills of various texts.
3. Improve advanced level thinking ability in general aptitude.
4. Develop emotional stability to tackle difficult circumstances.

Module:1	**Resume skills – Resume Template; Use of power verbs; Types of resume; Customizing resume**	**2 hours**

Structure of a standard resume, Content, color, font, Introduction to Power verbs and Write up, Quiz on types of resume, Frequent mistakes in customizing resume, Layout-Understanding different company's requirement, Digitizing career portfolio.

Module:2	**Interview skills – Types of interview; Techniques to face remote interviews and Mock Interview**	**3 hours**

Structured and unstructured interview orientation, Closed questions and hypothetical questions, Interviewers' perspective, Questions to ask/not ask during an interview, Video interview, Recorded feedback, Phone interview preparation, Tips to customize preparation for personal interview, Practice rounds.

Module:3	**Emotional Intelligence - L1 – Transactional Analysis; Brain storming; Psychometric Analysis; SWOT analysis**	**12 hours**

Introduction, Contracting, ego states, Life positions, Individual Brainstorming, Group Brainstorming, Stepladder Technique, Brain writing, Crawford's Slip writing approach, Reverse brainstorming, Star bursting, Charlette procedure ,Round robin brainstorming, Skill Test, Personality Test, More than one answer, Unique ways, SWOT analysis.

Module:4	**Quantitative Ability - L3–Permutation - Combinations; Probability; Geometry and menstruation; Trigonometry; Logarithms; Functions; Quadratic Equations; Set Theory**	**14 hours**

Counting, Grouping, Linear Arrangement, Circular Arrangements, Conditional Probability, Independent and Dependent Events, Properties of Polygon, 2D & 3D Figures, Area & Volumes, Heights and distances, Simple trigonometric functions, Introduction to logarithms, Basic rules of logarithms, Introduction to functions, Basic rules of functions, Understanding Quadratic Equations, Rules & probabilities of Quadratic Equations, Basic concepts of Venn Diagram.

Module:5	**Reasoning ability - L3 – Logical reasoning; Data Analysis and Interpretation**	**7 hours**

Syllogisms, Binary logic, Sequential output tracing, Crypto arithmetic, Data Sufficiency, Data Interpretation-Advanced, Interpretation tables, pie charts & bar chats.		
Module:6	**Verbal Ability - L3 – Comprehension and Critical reasoning**	**7 hours**
Reading comprehension, Para Jumbles, Critical Reasoning (a) Premise and Conclusion, (b) Assumption & Inference, (c) Strengthening & Weakening an Argument.		
	Total Lecture hours:	**45 hours**

Reference Books	
1.	Michael Farra and JIST Editors,(2011).Quick Resume & Cover Letter Book: Write and Use an Effective Resume in Just One Day. Jist Works, Saint Paul, Minnesota.
2.	Flage Daniel E, (2003).The Art of Questioning: An Introduction to Critical Thinking. Pearson, London.
3.	David Allen, (2015).Getting Things done: The Art of Stress-Free productivity. Penguin Books, New York City.
4.	SMART, (2018). Place Mentor 1st edition. Oxford University Press, Chennai.
5.	FACE, (2016).Aptipedia Aptitude Encyclopedia. Wileypublications, Delhi.
6.	ETHNUS, (2013).Aptimithra. McGraw-Hill Education Pvt Ltd, Bangalore.
Websites:	
1.	www.chalkstreet.com
2.	www.skillsyouneed.com
3.	www.mindtools.com
4.	www.thebalance.com
5.	www.eguru.ooo

Mode of Evaluation: Continuous Assessment Tests, Quizzes, Assignment, Final Assessment Test			
Recommended by Board of Studies	19-05- 2022		
Approved by Academic Council	No.66	Date	16-06-2022